

Vis 220

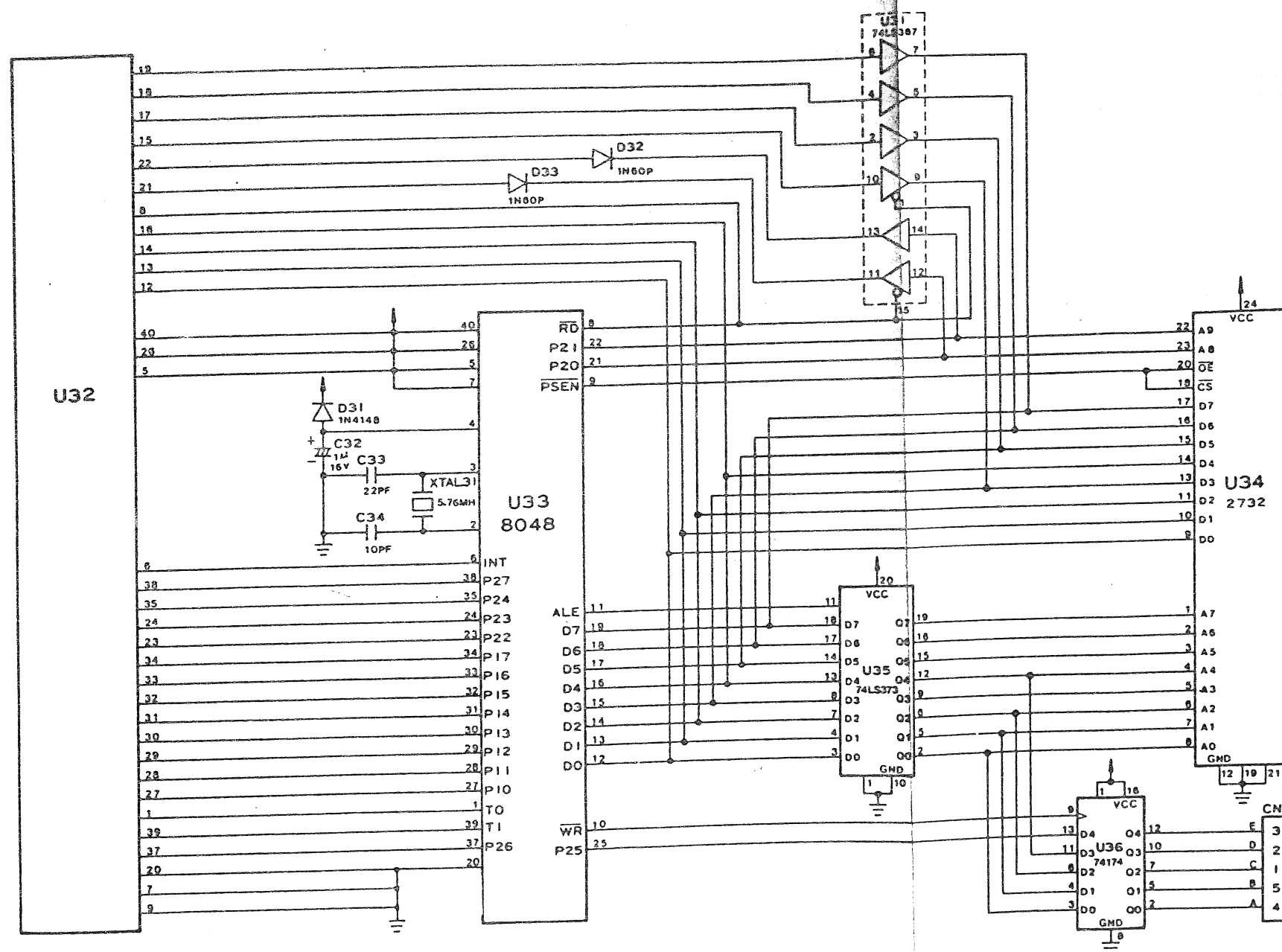


Figure E-2 (Sheet 1 of 2)
V220/240/241 Keyboard
(Daughter Board)

Schematic Diagrams E-5/E-6

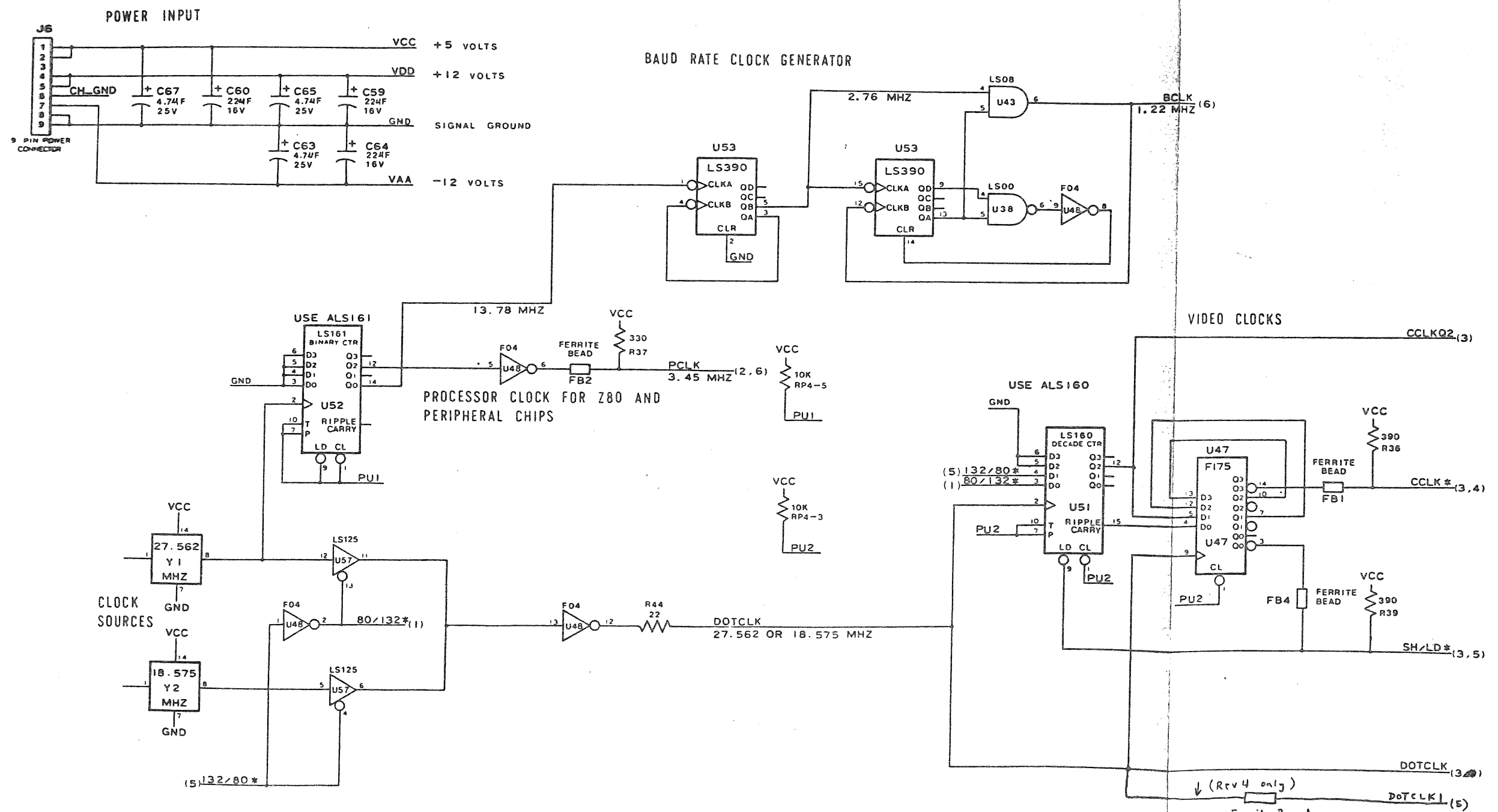


Figure E-3 (Sheet 1 of 6)
Logic Board Revision A
Clock Generation and
Power Input

VIDEO PROCESSOR AND CONTROLLER

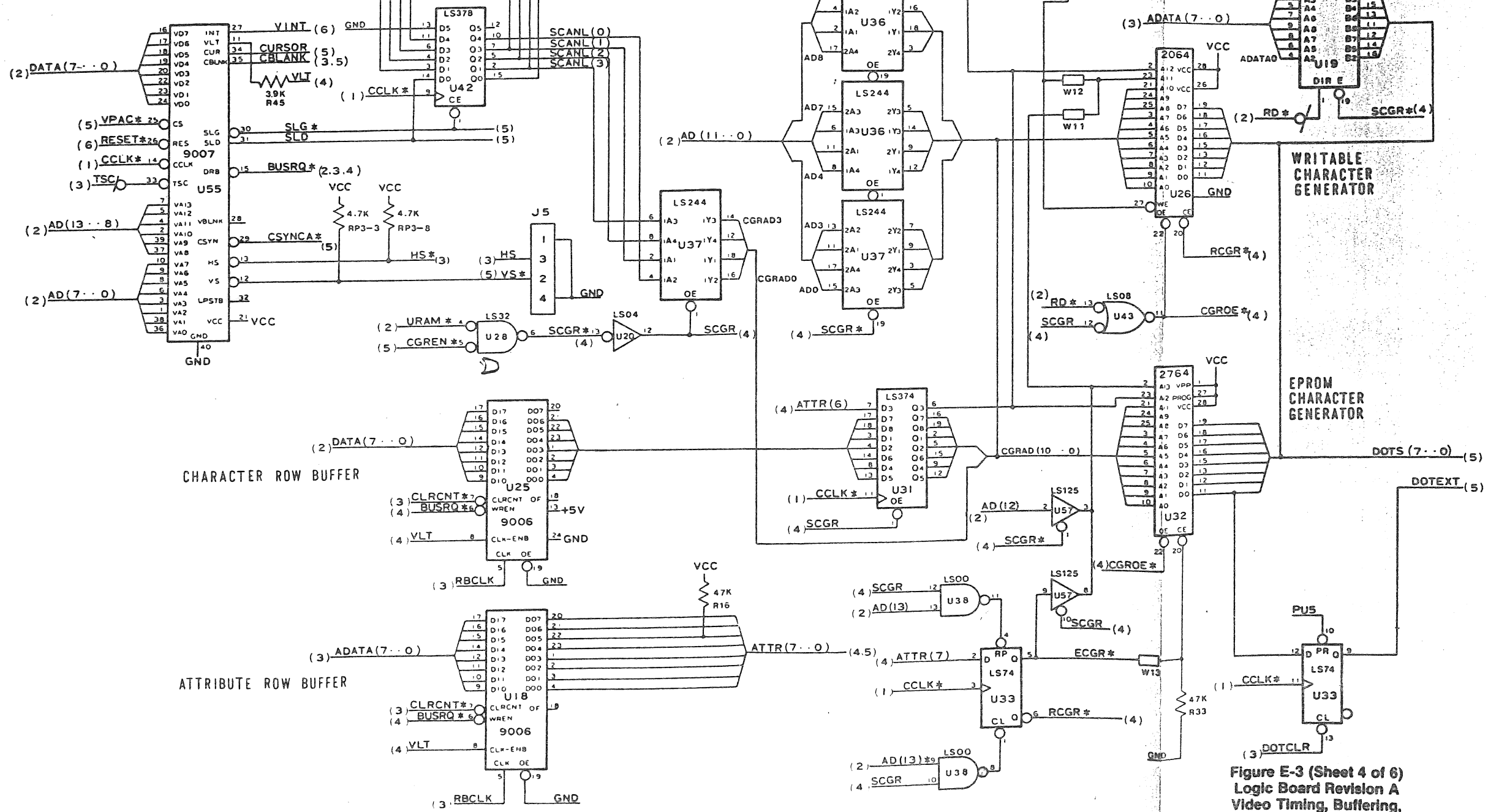
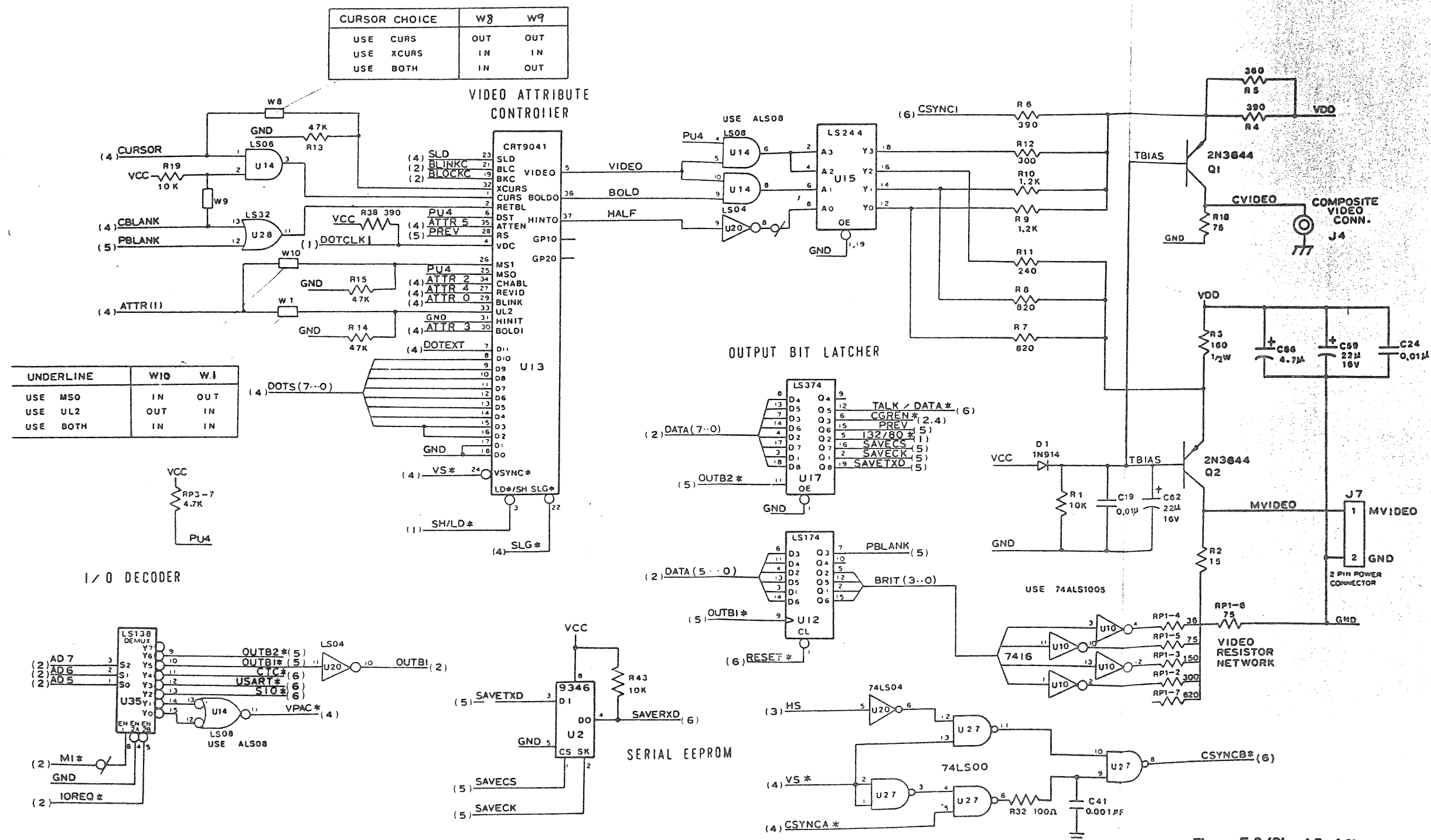


Figure E-3 (Sheet 4 of 6)
 Logic Board Revision A
 Video Timing, Buffering,
 Character Generation
 Schematic Diagrams E-15/E-16



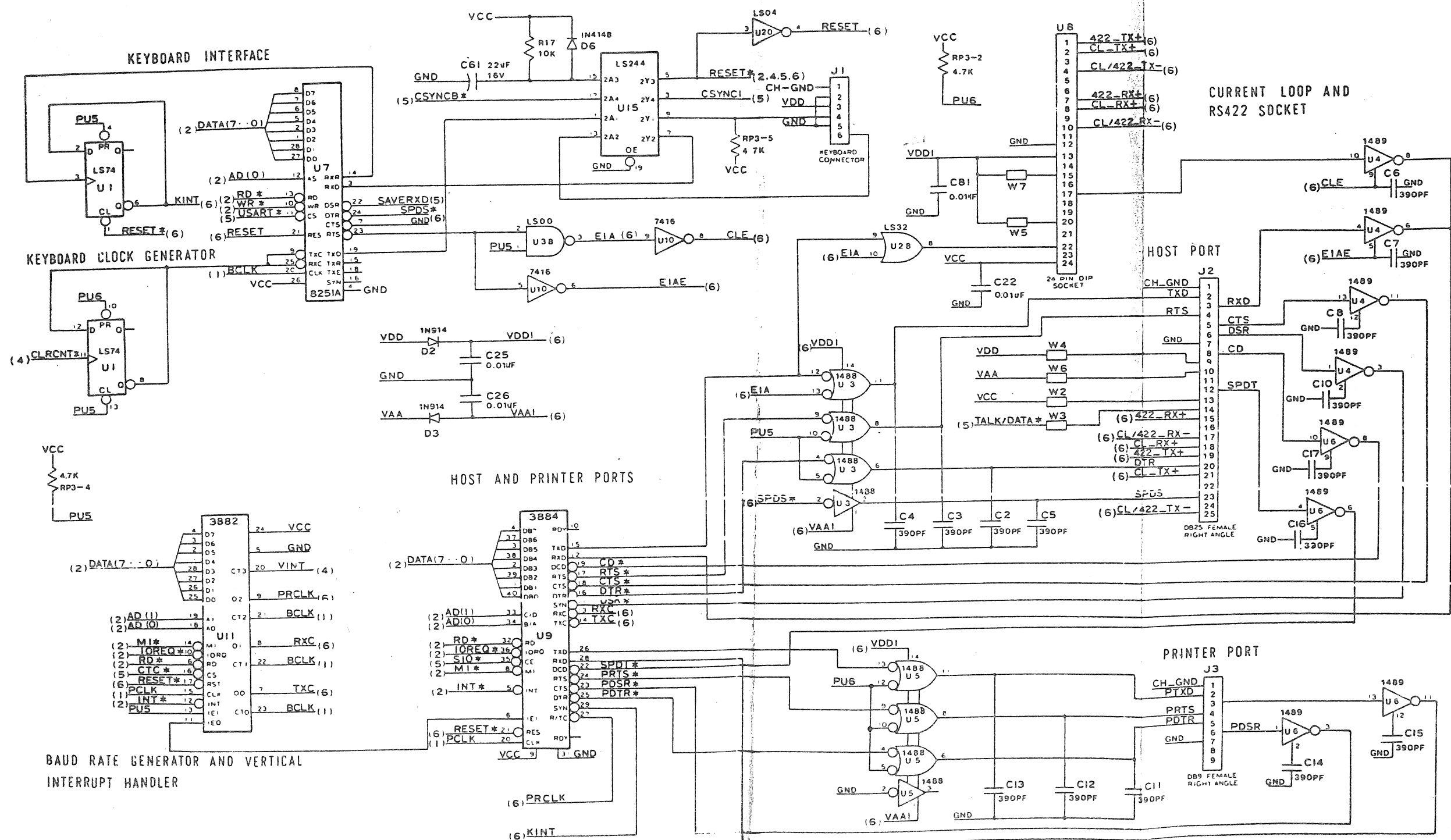


Figure E-3 (Sheet 6 of 6)
Logic Board Revision A
Host, Printer and Keyboard
Serial Channels

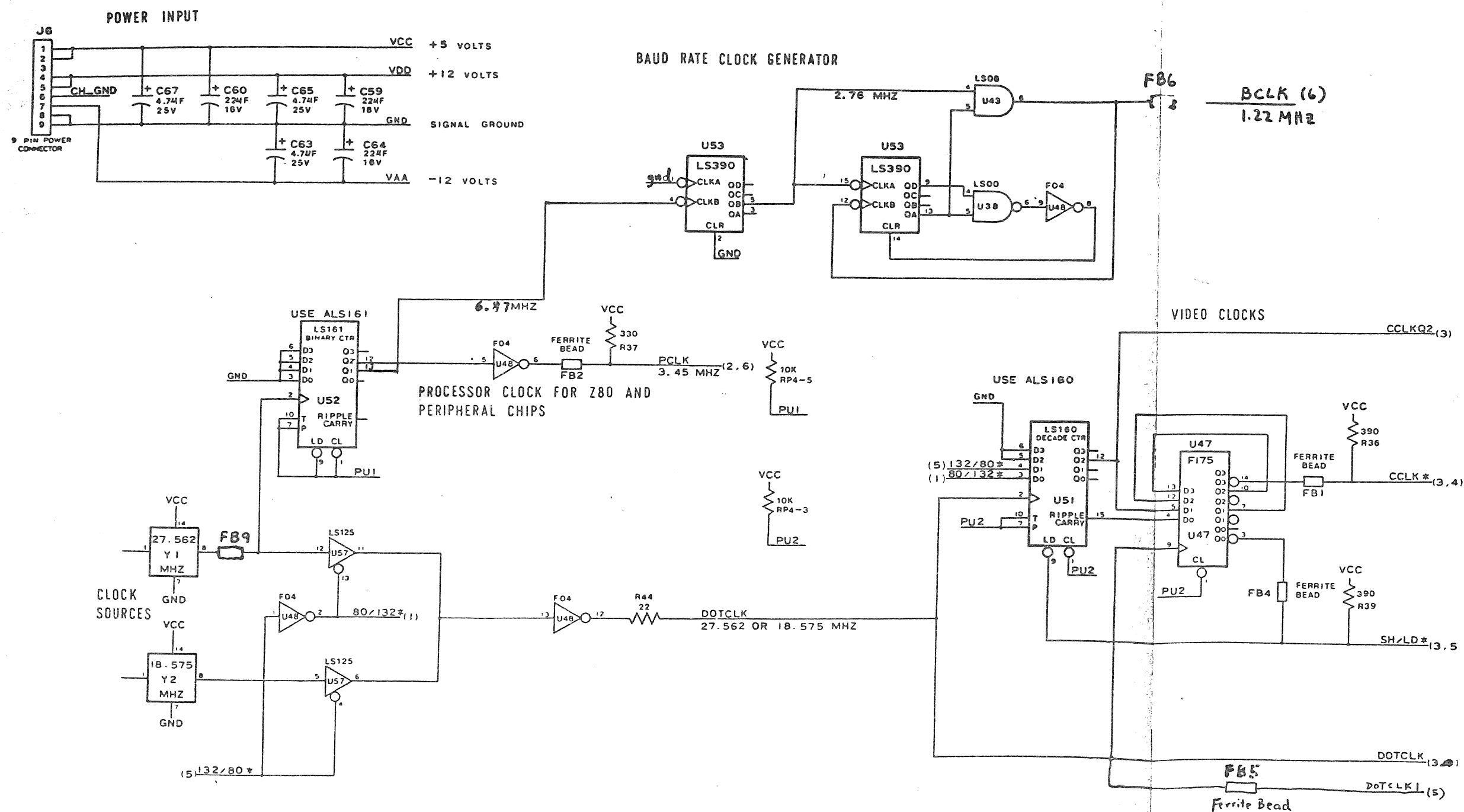
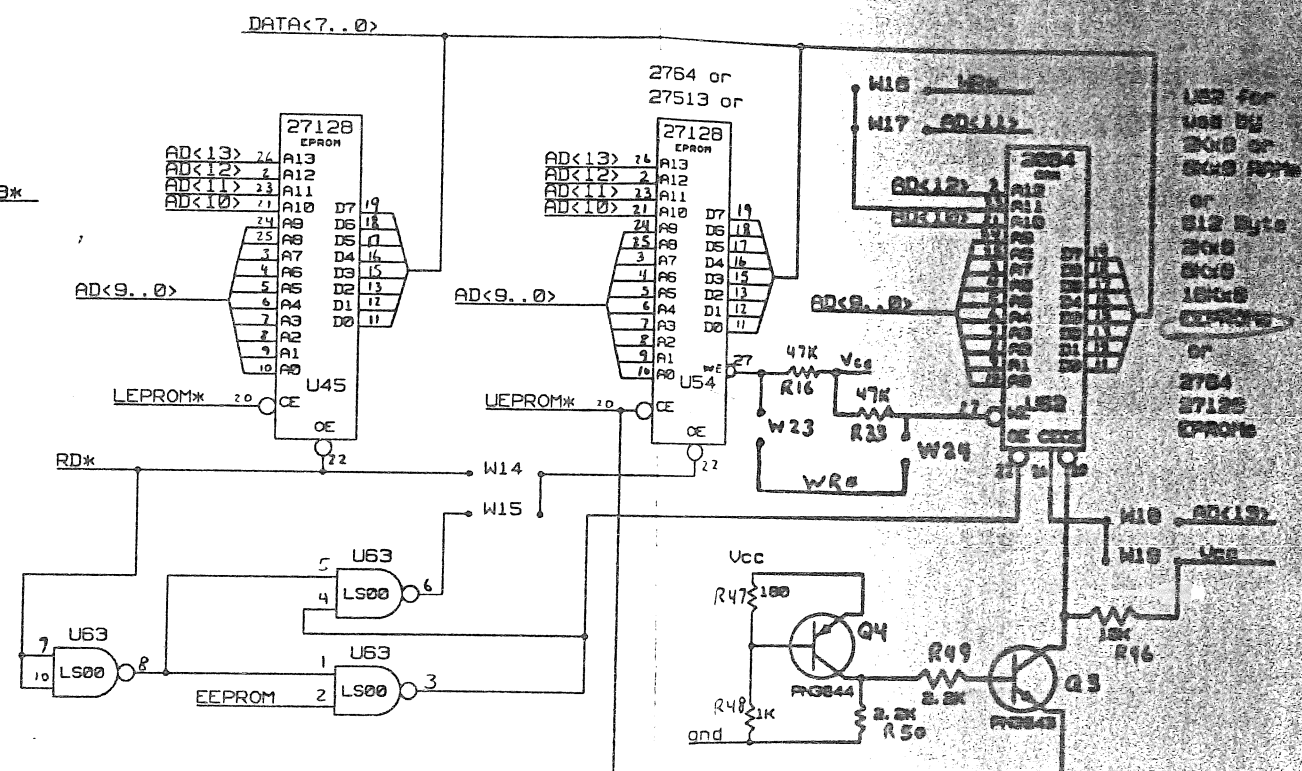
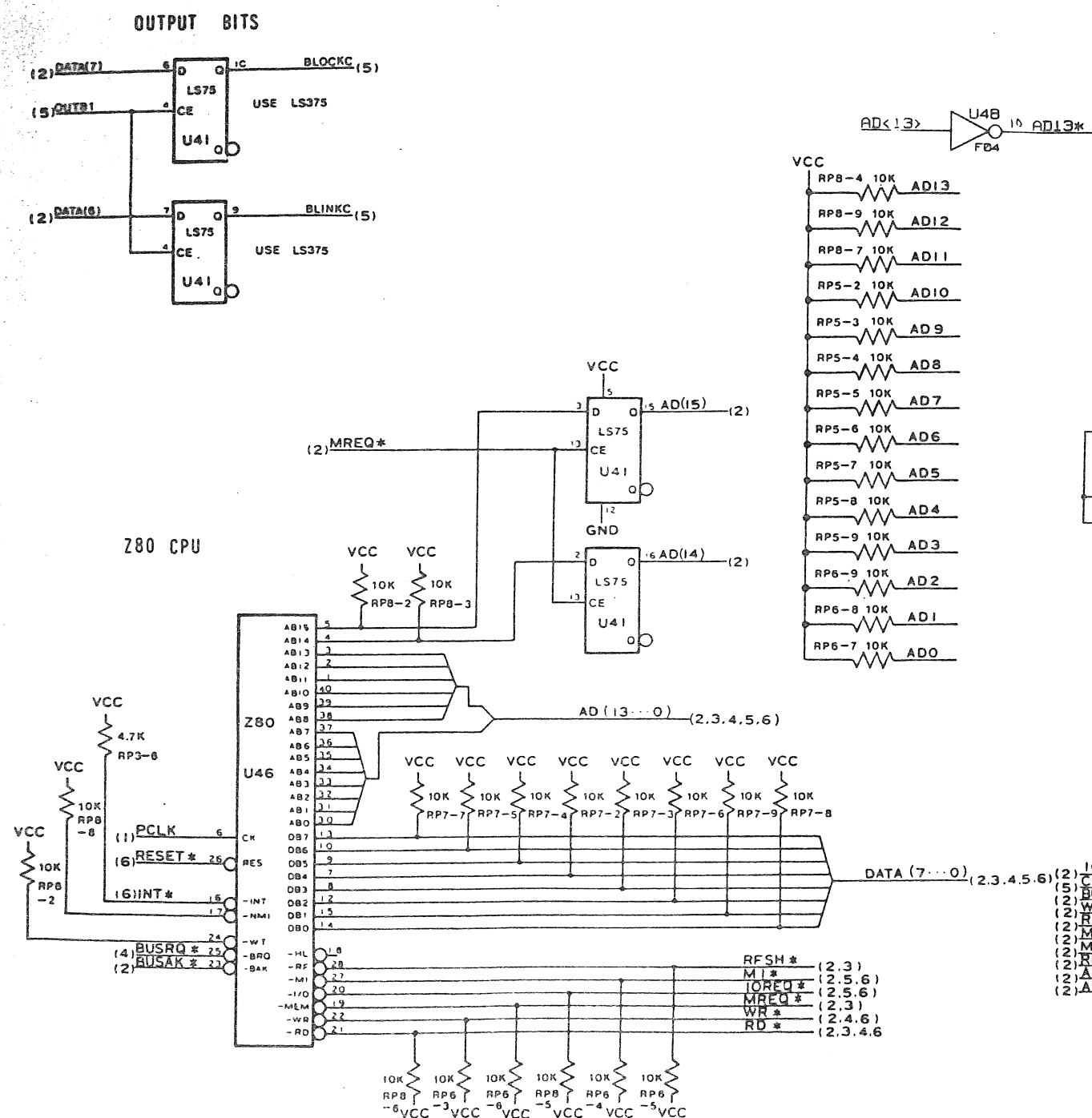


Figure E-4 (Sheet 1 of 6)
Logic Board Revision C
Clock Generation and
Power Input



PAL EQUATIONS

UEPROM* = AD15 AD14 RFSH* BUSAK* IOREQ* MT*
AD15 AD14 RFSH* BUSAK* MREQ*

LEPROM* = AD15 AD14 RFSH* BUSAK* IOREQ* MT*
AD15 AD14 RFSH* BUSAK* MREQ*

URAM* = AD15 AD14 RFSH* BUSAK* MREQ*

$$\text{RAMDIS*} = \text{MREQ*} + \overline{\text{MI*}}$$

URAMOE* = AD15 AD14 CGREN* RD* MREQ* + BUSAK*

URAMWR*- AD15 AD14 CGREN*MREQ* BUSAK*WR*

LRAMOE* = AD15 AD14 MREQ* RD* + BUSAK*

LRAMWR* = AD15 AD14 MREQ* BUSAK* WR*

Figure E-4 (Sheet 2 of 6)
Logic Board Revision C
Z80 Processor and Firmware

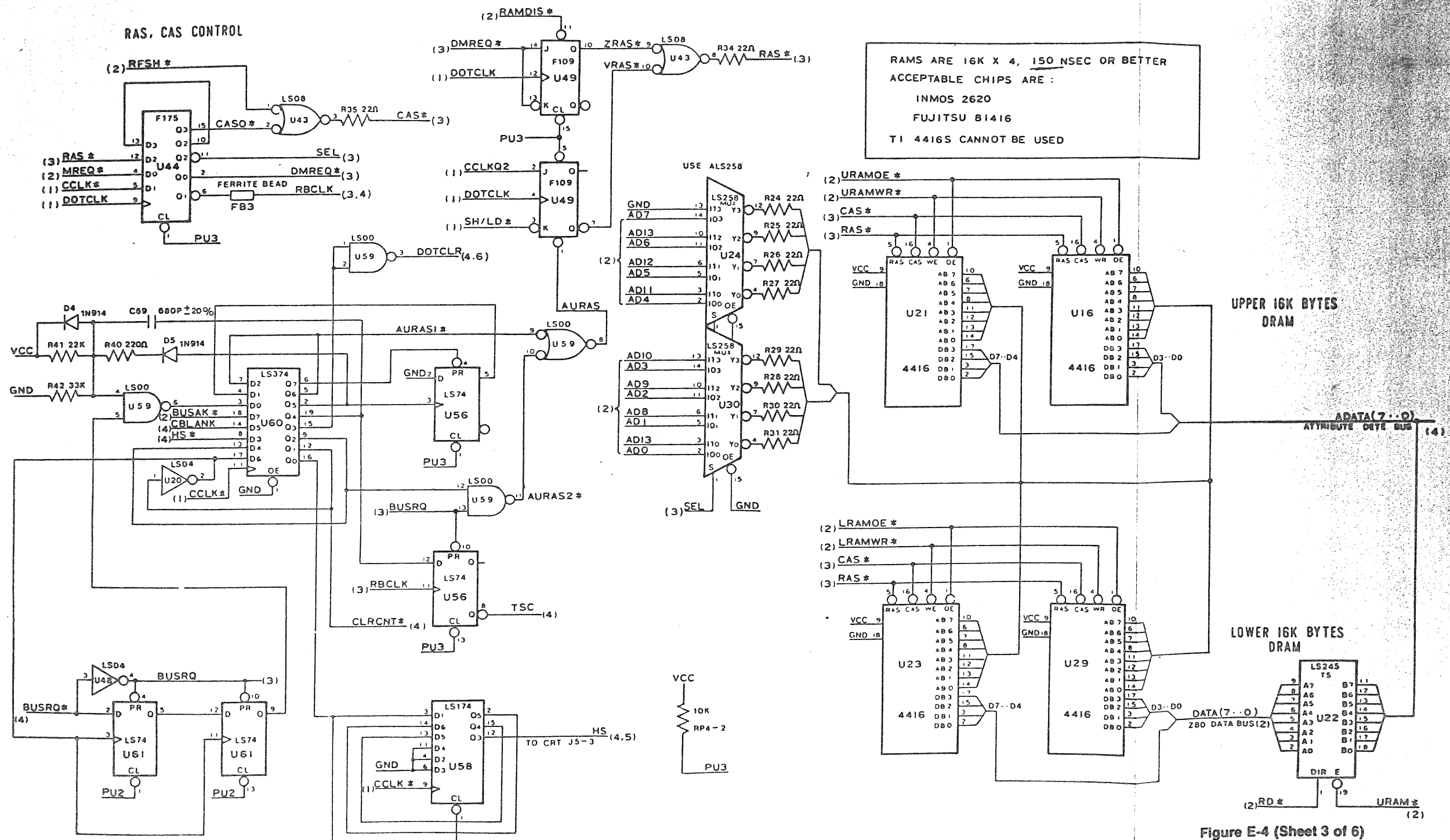
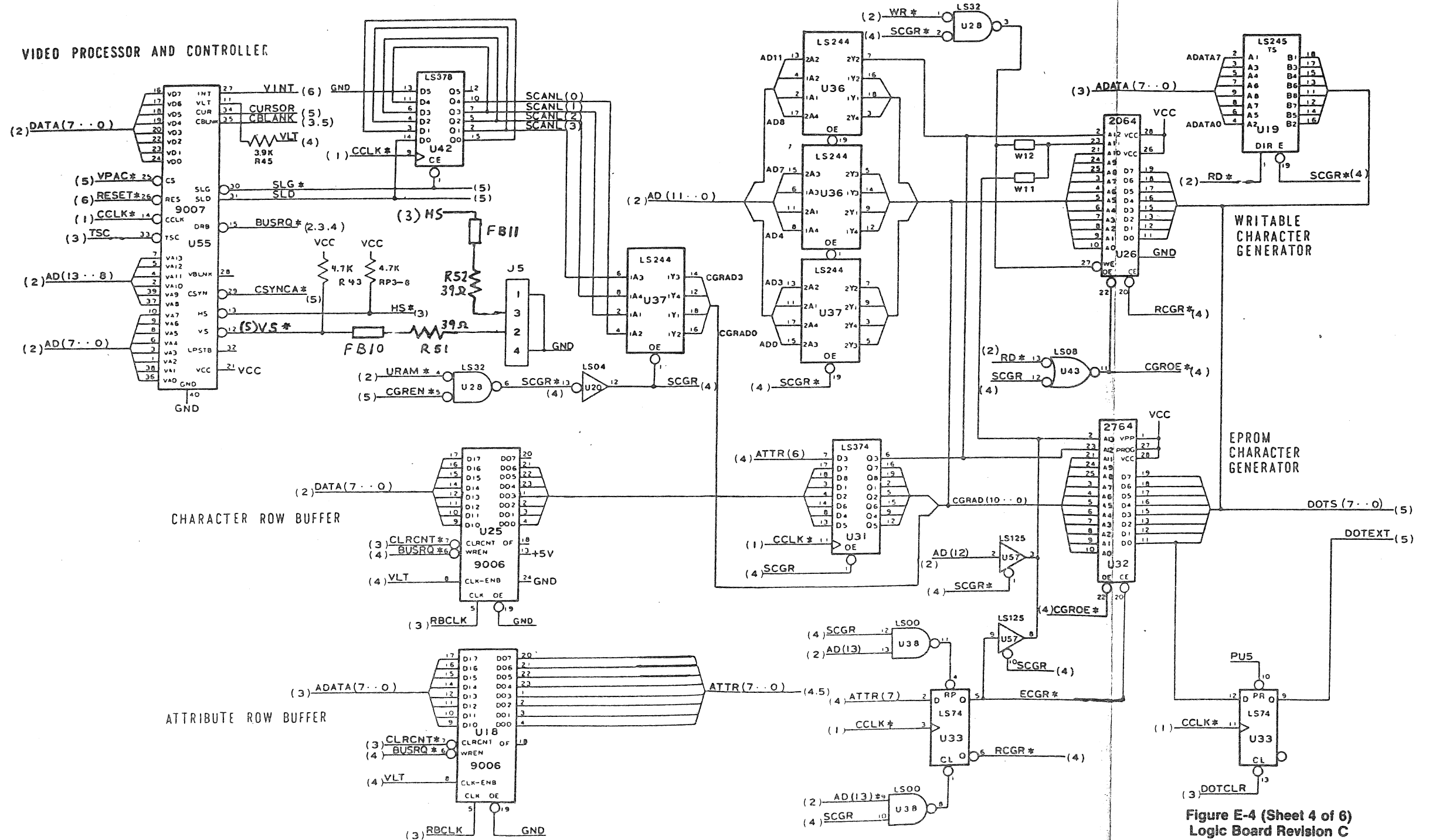


Figure E-4 (Sheet 3 of 6)
 Logic Board Revision C
 Dynamic RAM



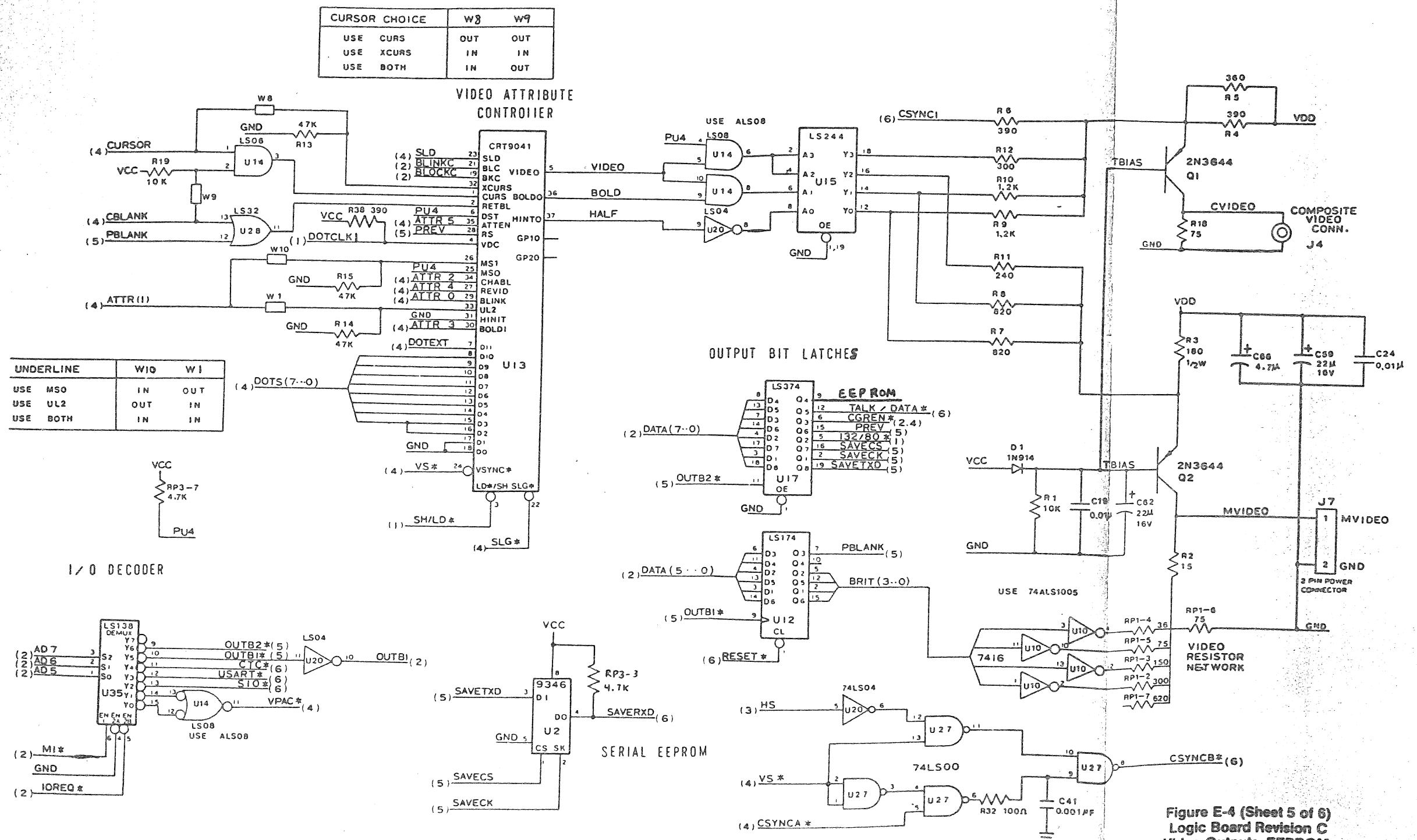


Figure E-4 (Sheet 5 of 6)
Logic Board Revision C
Video Outputs, EEPROM,
I/O Decoding and Buffers

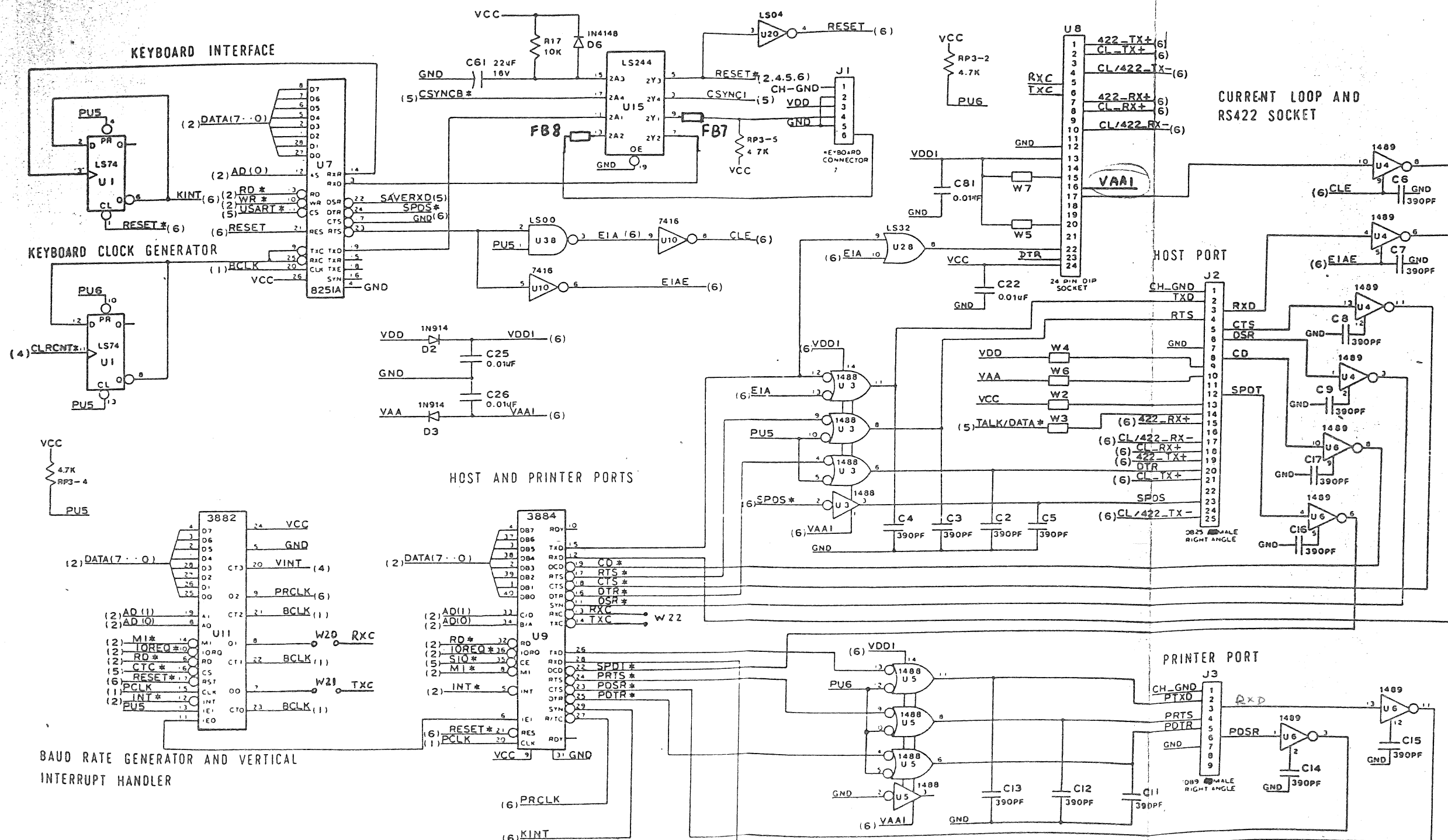
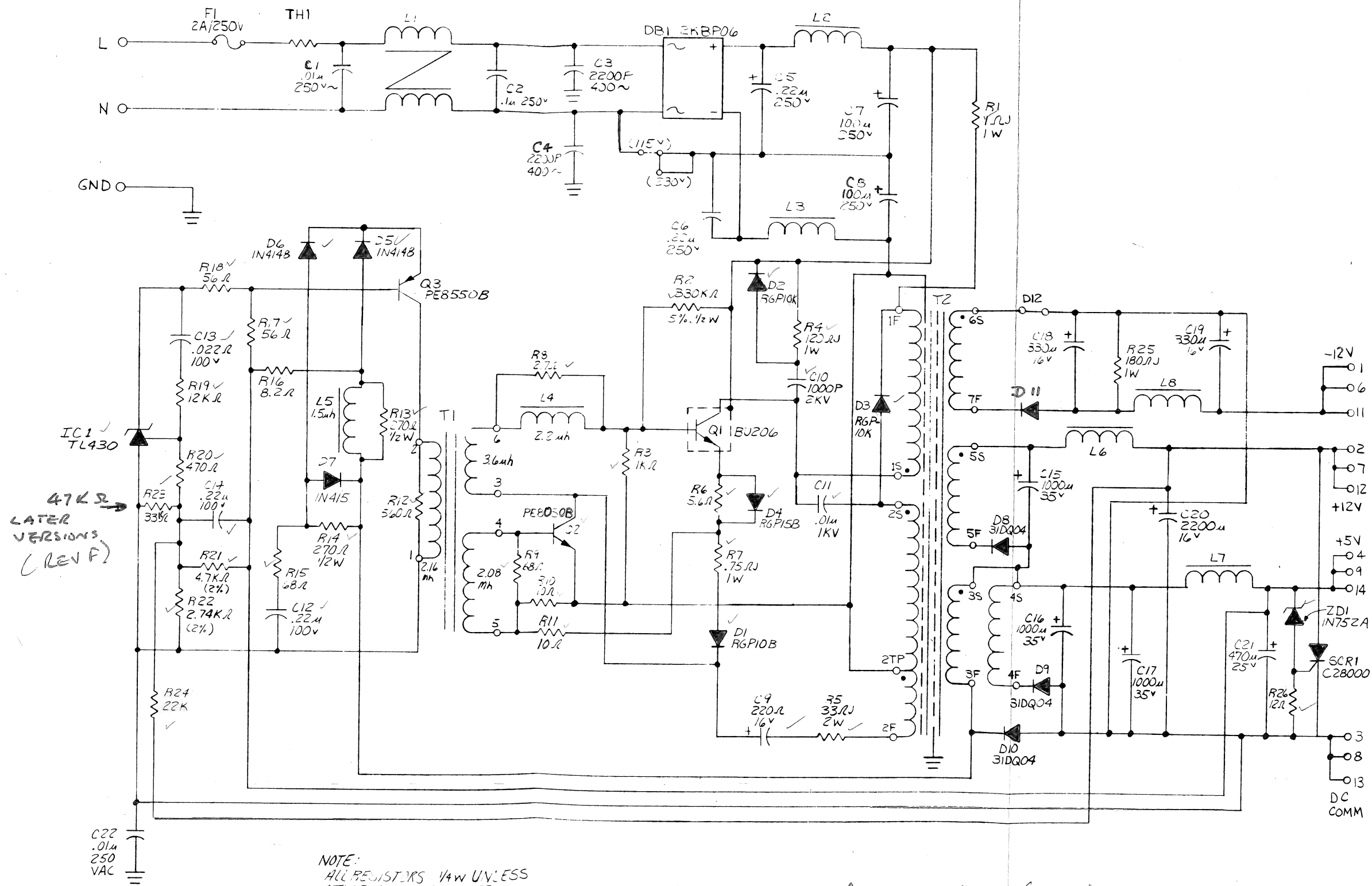
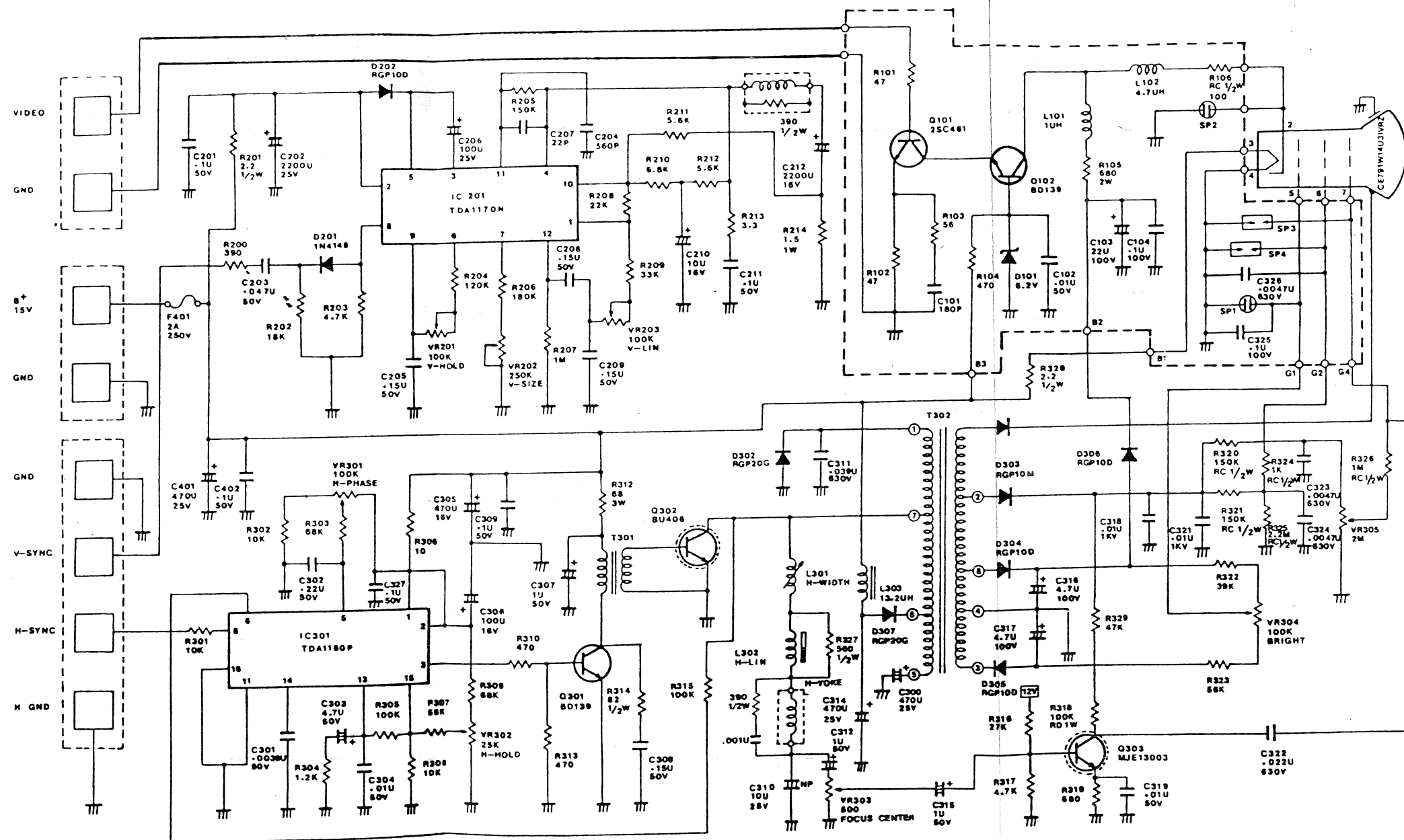


Figure E-4 (Sheet 8 of 6)
 Logic Board Revision C
 Host, Printer and Keyboard
 Serial Channels
 Schematic Diagrams E-31/E-32



(Q₂) 2N2102 WILL DO

Figure E-1 (Sheet 1 of 1)
42 Watt Switching Power Supply



NOTE *
 MONITOR BOARD IS THE SAME AS ESPRIT 6310
 EHT TRANSFORMER PART NO 1-482-024-01 IS
 A SEPARATE ITEM.

Figure E-5 (Sheet 1 of 1)
 V220/V240
 Monitor Schematic