

digital

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Engineering Drawings

Digital Equipment Corporation

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CUSTOMER PRINT SET INDEX

THIS IS PRINT SET

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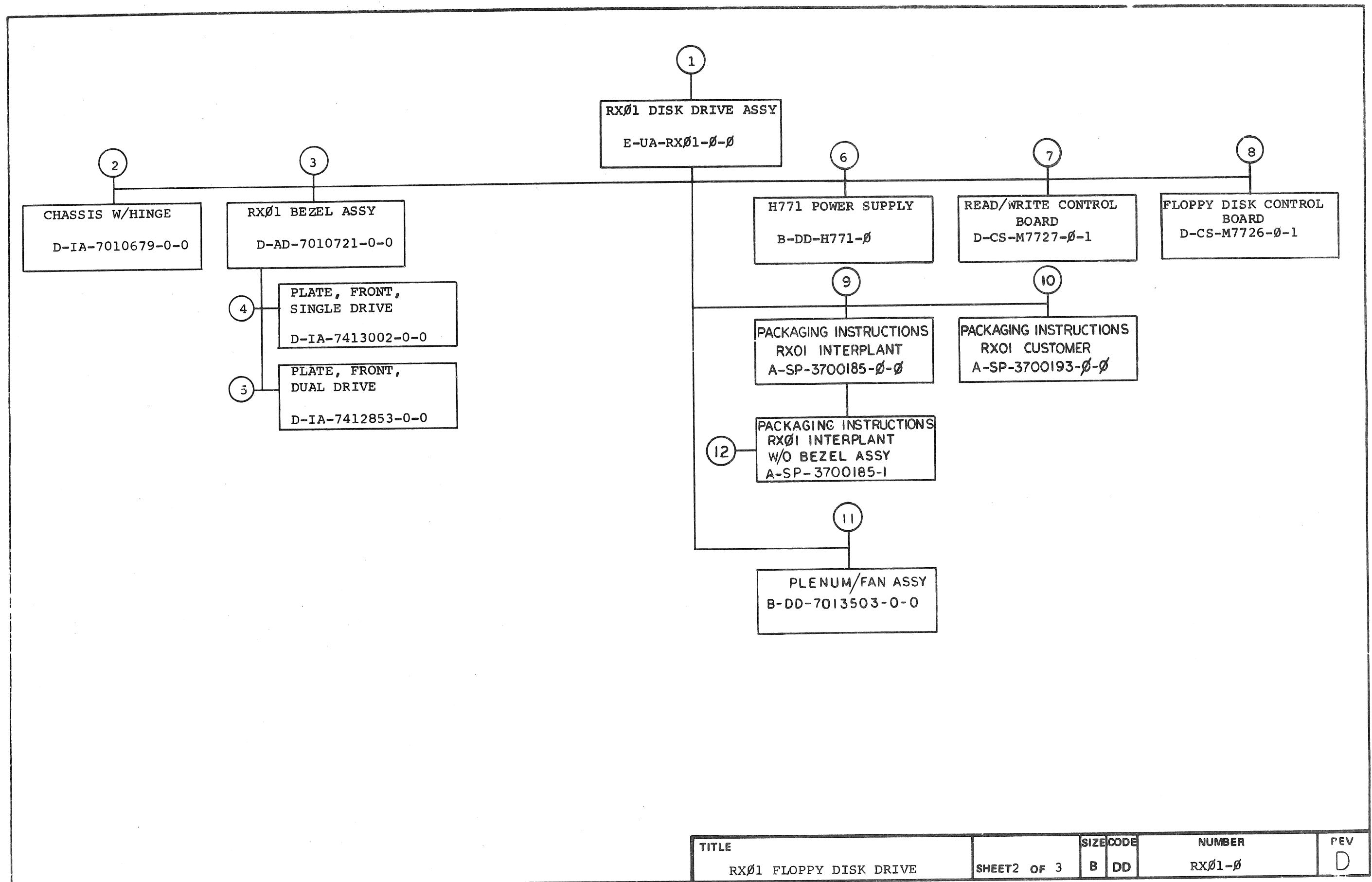
SEQUENCE

SEQUENCE

RX01 FLOPPY DISK DRIVE
FLOPPY DISK CONTROL BOARD
RX01 FIRMWARE LISTING
READ/WRITE CONTROL BOARD
H771 POWER SUPPLY
PLENUM/FAN ASSY.

B-DD-RXØ1-Ø
D-CS-M7726-Ø-1
K-SP-RXØ1-O-2
D-CS-M7727-Ø-1
B-DD-H771-Ø
B-DD-7Ø135Ø3-Ø

[illegible][illegible]



TITLE	SHEET	OF	SIZE	CODE	NUMBER	REV
RX01 FLOPPY DISK DRIVE	2	3	B	DD	RX01-0	D

MECHANICAL						ELECTRICAL									
CUSTOMER PRINT SET	MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE	CUSTOMER PRINT SET	MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
		1	E-UA-RX01-0-0		5	RX01 FLOPPY DISK DRIVE ASSY		X		1	B-DD-RX01-0	#	3	RX01 FLOPPY DISK DRIVE	
			A-PL-RX01-0-0		2	RX01 FLOPPY DISK DRIVE ASSY(PL)									
			E-IA-7412666-0-0		1	COVER, TOP									
			D-IA-7010646-0-0		1	CABLE, EXTENSION, RX01									
			C-IA-7008612-0-0		1	CABLE, KEYBOARD									
			D-UA-BC05L-0-0		1	CABLE, JUMPER		C							
			D-IA-7010696-0-0		1	HARNESS, VOLTAGE VARIATION									
			C-MD-7413350-0-0		1	BRACKET, SHIPPING, RX01									
			C-MD-7409479-0-0		1	PLATE, PRESSURE									
			C-MD-5509081-0-0		1	PANEL, LIGHT (RX01)									
		2	D-IA-7010679-0-0		1	CHASSIS W/HINGE									
			E-IA-7412665-0-0		1	CHASSIS, FLEXIBLE DISK DRIVE									
			C-MD-7413236-0-0		1	HINGE, LOGIC									
		3	D-AD-7010721-0-0		1	RX01 BEZEL ASSY		X		7	D-CS-M7727-0-1	#	6	READ/WRITE CONTROL BOARD	
			E-MD-7412664-0-0		1	BEZEL, RX01					D-IA-5011370-0-0		1	ETCHED CIRCUIT BOARD (M7727)	
			A-DC-7413429-0-0		1	LOGO, RX01									
		4	D-IA-7413002-0-0		1	PLATE, FRONT, SINGLE DRIVE		X		8	D-CS-M7726-0-1	#	9	FLOPPY DISK CONTROL BOARD	
			C-SS-7413002-0-1		1	SILK SCREEN, SINGLE DRIVE					A-SP-M7726-0-7		3	ACCEPTANCE TEST PROCEDURE	
		5	D-IA-7412853-0-0		1	PLATE, FRONT, DUAL DRIVES				9	A-SP-3700185-0-0			PACKAGING INST. INTERPLANT	
			C-SS-7412853-0-1		1	SILK SCREEN, DUAL DRIVE					A-PS-9905710-0-0			REGULAR SLOTTED CARTON	
											A-PS-9905711-0-0			ONE PIECE FOLDER	
											A-PS-9905712-0-0			PLYWOOD SUPPORT FIXTURE	
											A-PS-9905713-0-0			SCORED SHEET	
											A-PS-9905729-0-0			CARTON SEALING TAPE	
		6	B-DD-H771-0	*	3	H771 POWER SUPPLY				10	A-SP-3700193-0-0			PACKAGING INST. CUSTOMER	
											A-PS-9905741-0-0			FULL TELESCOPE CAP	
											A-PS-9905740-0-0			FOAM PAD	
											A-PS-9905739-0-0			LAMINATED BUILDUP	
											A-PS-9905734-0-0			PLASTIC STRAPPING	
		11	B-DD-7013503-0-0		3	PLENUM/FAN ASSY									

CUSTOMER PRINT SET CODES

X = PRINT OF DOCUMENT INCLUDED IN PRINT SET

C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT

S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE

RX01 FLOPPY DISK DRIVE

SHEET 3 OF 3

SIZE CODE

B DD

NUMBER

RX01-0

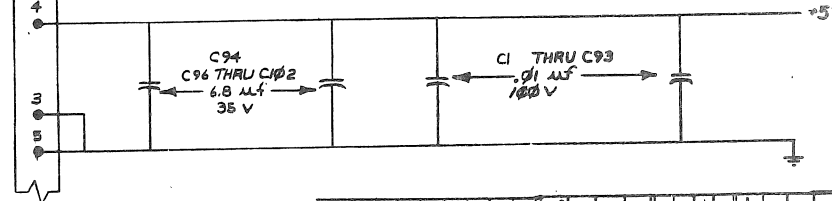
REV

D

1. ① REPRESENTS A $\frac{1}{8}$ DIA PAD LOCATED ON SIDE 2
2. UNLESS OTHERWISE SPECIFIED
 - A. ALL RESISTORS ARE $\frac{1}{4}W$, $\pm 5\%$
 - B. ALL UNUSED PINS FOR J1 ARE TIED TO GND
3. INSTALL JUMPER W1 AFTER MODULE TEST
4. MOUNT E67 $\frac{1}{4}$ " ABOVE SURFACE OF MODULE



— SEE NOTE 4

digital

TITLE FLOPPY DISK
CONTROLLER

SIZE	CODE	NUMBER
D	CS	M 7726-Ø-1
UNIT		

SEMICONDUCTOR CONVERSION CHART

SHEET /
2

SIZE	CODE	NUMBER	REV.
D	CS	M7726-Ø-1	H

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PARTS LIST				
QTY	REF	DESIGNATION	DESCRIPTION	PART NO.
D	REF		X-Y COORDINATE HOLE LOCATION	KCO-M7726-0-4 1
REF			ASSY/DEILLING HOLE LAYOUT	D-AH-M7726-0-5 2
REF			MODULE ECO HISTORY	B-MH-M7726-0-6 3
1			ETCHED CIRCUIT BOARD	5011390 4
1	J3		RECEP 36 PIN (BEWOEK)	B-MD-5509 07-1 5
1	J2		I.C. SOCKET, 16 PIN	1211813-02 6
			GOLD, LOW PROFILE	
1	A37		RES 10K 1/4W 5% CC	1300479-00 7
3	C 94, C96 - C102		CAP 6.8 uF 35V 10% 5-TANT	1005306-00 8
93	C1 - C93		CAP .01 uF 50V AXIAL CER	1001610-00 9
1	C95		CAP 12 PF 100V 5%	1002087-00 10
3	D1 - D3		DIODE 1N4004	1105796-00 11
1	D4		DIODE 1N746A 3.3V 5%	1104860-00 12
1	R 39		RES 100 1/2W 5% C.C	1300228-00 13
3	J4		HEADER, 2 PIN (MALE)	1212204-00 14
8	R2, R4, R6, R8, E10		RES 470 1/4W 5% CC	1300316-00 15
	R12, R14, R16			
8	R27, R29, R31, R47, R52		RES 390 1/4W 5% CC	1300309-00 16
	R43, R41, R45			
5	R1, R49 - R51, R57		RES 3K 1/4W 5% CC	1300432-00 17
5	R26, R28, R30, R38		RES 180 1/4W 5% CC	1301322-00 18
	R42, R44, R46, R48, R53			
8	R3, R5, R7, R9, E11		RES 820 1/4W 5% CC	1301775-00 19
	R13, R15, R17			
1	R35		RES 300 1/4W 5% CC	1301425-00 20
8	R18 - R25		RES 2K 1/4W 5% CC	1302358-00 21
1	R34		RES 261 1/4W 1% MF	1302873-00 22
1	R36		RES 287 1/4W 1% MF	1305124-00 23
1	R40		RES 3.2K 1/4W 5% CC	1303179-00 24
3	R54 - R56		RES 1K 1/4W 5% CC	1300365-00 25
1	Q2		TRANS MXA805	1510705-00 26
1	Q1		TRANS MXA855	1510706-00 27
	E19, E20, E21, E29		I.C. 7474	1905547-00 28
5	E40			
3	E9, E57, E59		I.C. 7400	1905575-00 29
2	E43, E60		I.C. 7410	1905576-00 30
1	E75		I.C. 7450	1905580-00 31
1	E55		I.C. 74H20	1905635-00 32
1	E54		I.C. 7402	1909004-00 33
2	E68, E72		I.C. 74H00	1909056-00 34
2	E56, E70		I.C. 74H11	1909267-00 35
5	E58, E69, E70, E79, E82		I.C. 74H74	1909667-00 36
2	E64, E76		I.C. 7404	1909686-00 37
1	E39		I.C. 74154	1909701-00 38
2	E1, E2		I.C. 8881	1909705-00 39
1	E61		I.C. 74H04	1909931-00 40
2	E74, E92		I.C. 7486	1910011-00 41
4	E88, E89, E90, E91		I.C. 74193	1910018-00 42
2	E27, E37		I.C. 8266	1909934-00 43
1	E22		I.C. 7442	1910046-00 44
1	E65		I.C. 7437	1910091-00 45
1	E49		I.C. 74150	1910153-00 46
2	E11, E12		I.C. 7408	1910155-00 47
2	E47, E48		I.C. 7489	1910396-00 48
1	E50		I.C. 74H106	1910408-00 49
3	E80, E81, E87		I.C. 74H103	1910409-00 50
1	E42		I.C. 74123	1910436-00 51

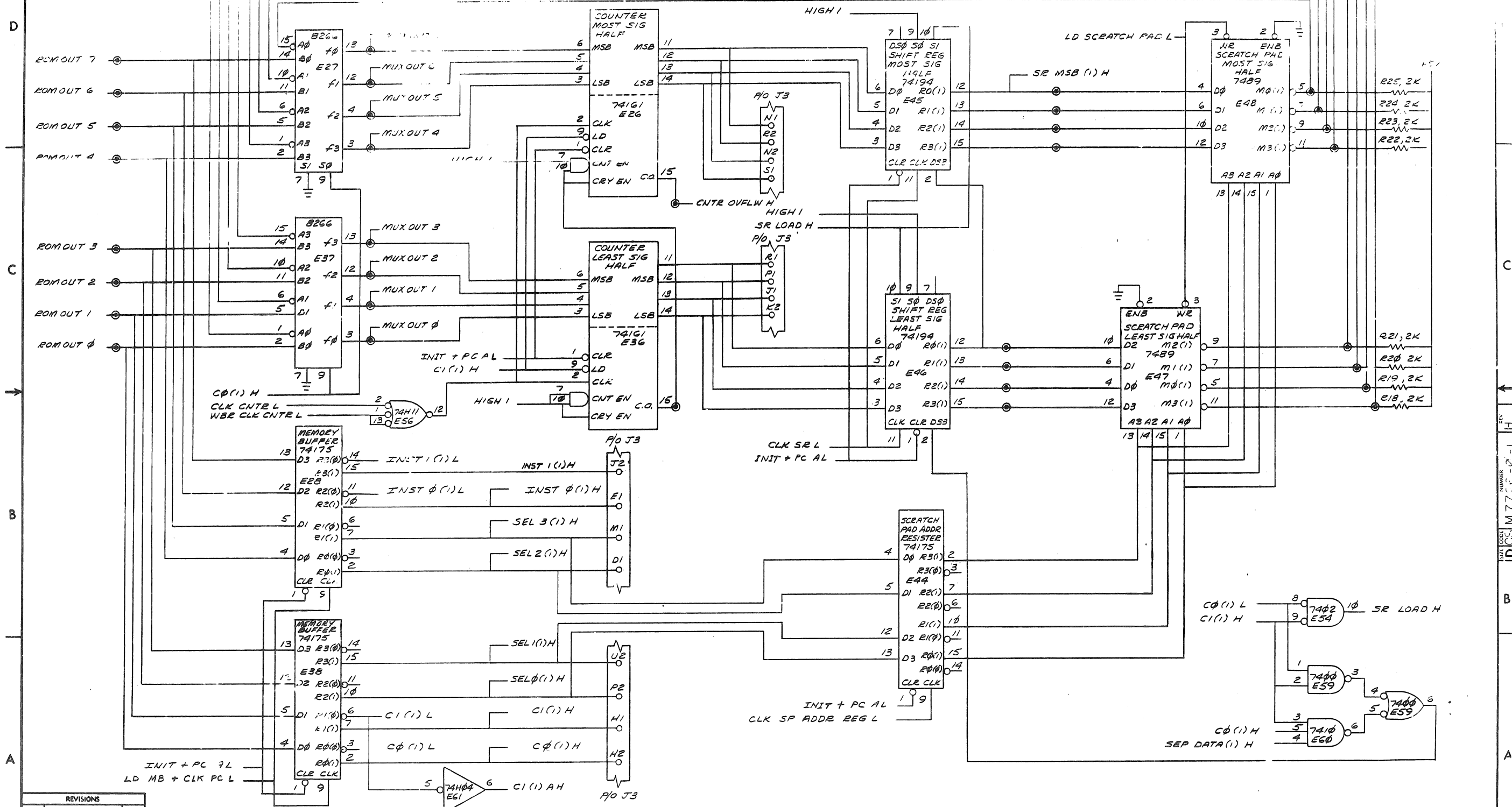
REVISIONS		
CHK	CHANGE NO.	REV.

PARTS LIST				
REF	DESIGNATION	DESCRIPTION	PART NO.	ITEM
2	E45, E46	I.C. 74194	1910623-00	52
8	E23, E24, E25, E26	I.C. 74161	1910650-00	53
	E30, E31, E32, E36			
3	E84, E85, E86	I.C. 74174	1910652-00	54
1	E53	I.C. 7427	1910878-00	55
3	E28, E38, E44	I.C. 74175	1910651-00	56
2	E10, E66	I.C. 8640	1911469-00	57
1	E33	I.C. 2102 650 NS	2111318-02	58
				59
6	E35, E39, E62, E63	SPARE I.C. SPACES		60
	E73, E83			
1	E67	CRYSTAL OSCILLATOR 20MHZ	1811660-00	61
4	E41, E71, E93, E52	I.C. 74574	1910544-00	62
1	E51	I.C. 74H10	1909057-00	63
1	E77	I.C. 74H40	1908886-00	64
				65
A/R		30 AWG SOLID WIRE (VRL)	9103740-00	66
1	J1	CONN 40 PIN ET ANG HDR	1209941-02	67
1	(J1)	LATCH, LEFT FOR ET ANG HDR	1209941-03	68
1	(J1)	LATCH, RIGHT FOR ET ANG HDR	1209941-04	69
1	E13	I.C. 256 X 4 ROM FLD0L	23111A2	70
1	E3	I.C. 256 X 4 ROM FLD0H	23421A2	71
1	E14	I.C. 256 X 4 ROM FLD1L	23257A2	72
1	E4	I.C. 256 X 4 ROM FLD1H	23258A2	73
1	E15	I.C. 256 X 4 ROM FLD2L	23115A2	74
1	E5	I.C. 256 X 4 ROM FLD2H	23116A2	75
1	E16	I.C. 256 X 4 ROM FLD3L	23117A2	76
1	E6	I.C. 256 X 4 ROM FLD3H	23118A2	77
1	E17	I.C. 256 X 4 ROM FLD4L	23259A2	78
1	E7	I.C. 256 X 4 ROM FLD4H	23260A2	79
1	E18	I.C. 256 X 4 ROM FLD5L	23121A2	80
1	E8	I.C. 256 X 4 ROM FLD5H	23122A2	81
1	R33	RES 150 1/4W 5% CC	1300250-00	82

SPARE I.C. GATES			
TYPE	LOCATION	PINS	DESCRIPTION
74H04	E61	1,2	INVERTER
7404	E64	12,13	INVERTER
7404	E76	12,13	INVERTER
7408	E11	1,2,3,4,9,10	2 INPUT AND
74H00	E72	1,2,3,4,5,6,9,10	2 INPUT NAND
7437	E65	8,9,10	2 INPUT NAND BUFFER
8881	E2	8,9,10	2 INPUT NAND G.C.
74H10	E51	3,4,5,6	3 INPUT NAND
74H40	E77	1,2,4,5,6	4 INPUT NAND BUFFER
7402	E84	4,5,6	2 INPUT NOR
8640	E66	2,6,7,11,12,13,34,5	2 INPUT NOR ACVR
7427	E53	1,2,12,13	3 INPUT NOR
7486	E92	7,56	2 INPUT XOR
7486	E74	1,2,3,4,56	2 INPUT XOR
74574	E93	1,2,3,4,5,6	D TYPE FLIP FLOP
74H106	E50	1,2,3,4,14,15,16	J K FLIP FLOP
74123	E42	1,2,3,4,13,14,15	ONE SHOT

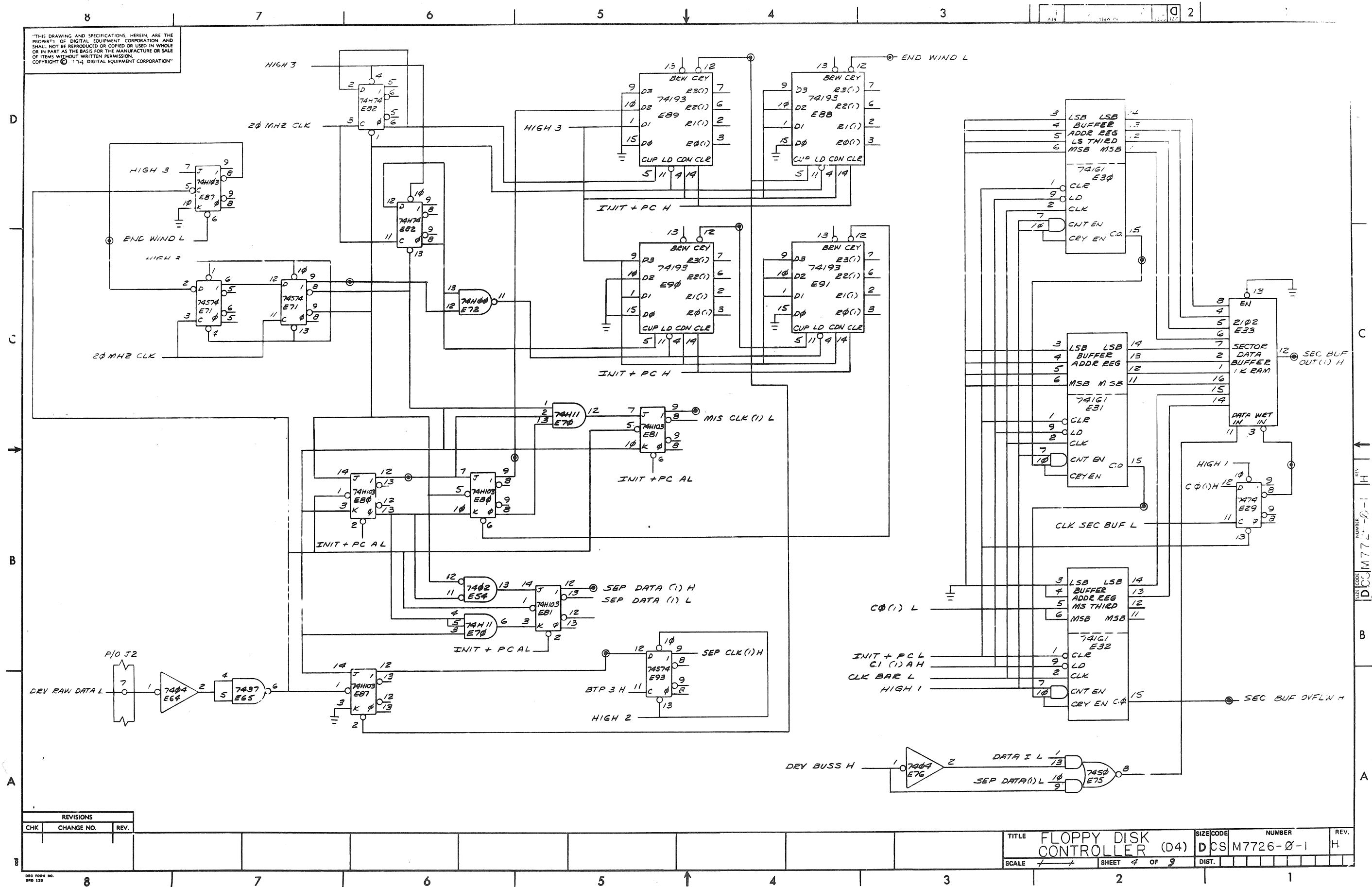
ALLOWABLE SUBSTITUTIONS				
PREFERRED			REPLACEMENT	
TYPE	ITEM #	P.N.	TYPE	P.N.
7489	48	1910396-00	3101A	1910653-00
7489	48	1910396-00	8225	1911162-00

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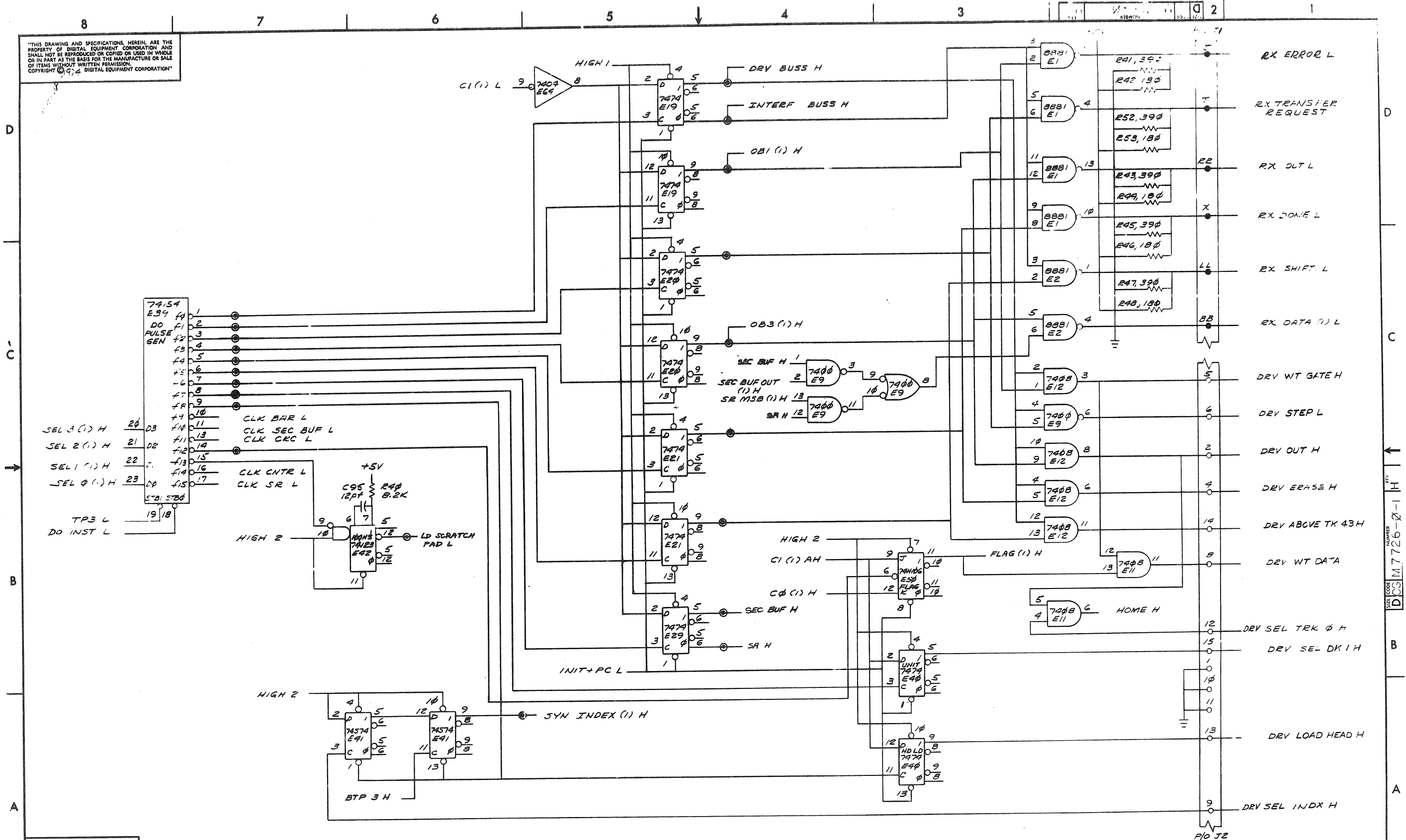


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		FLOPPY DISK	SIZE CODE	NUMBER	REV.
		CONTROLLER (D3)			
SCALE		SHEET 3 OF 9	DIST.		

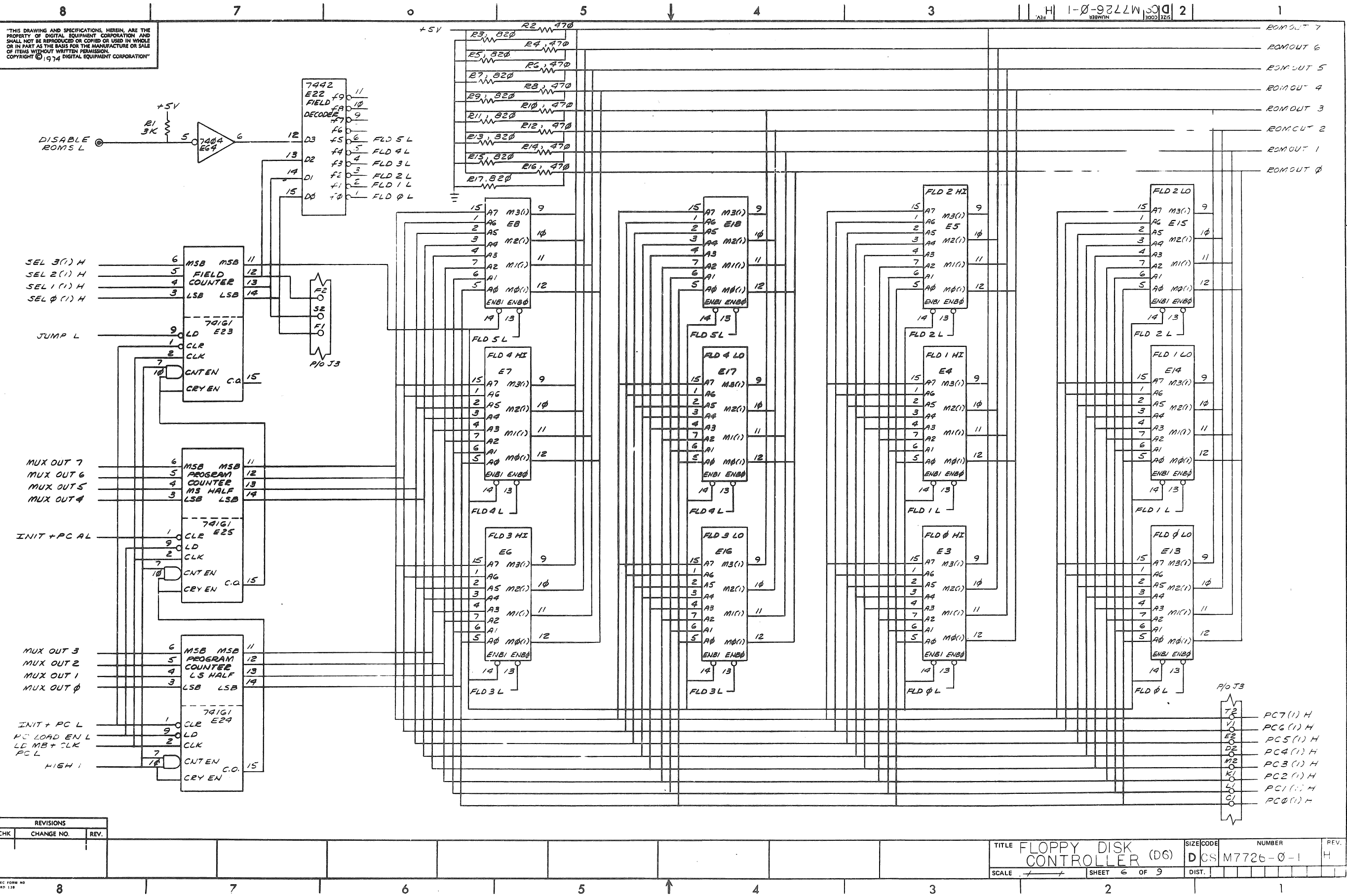


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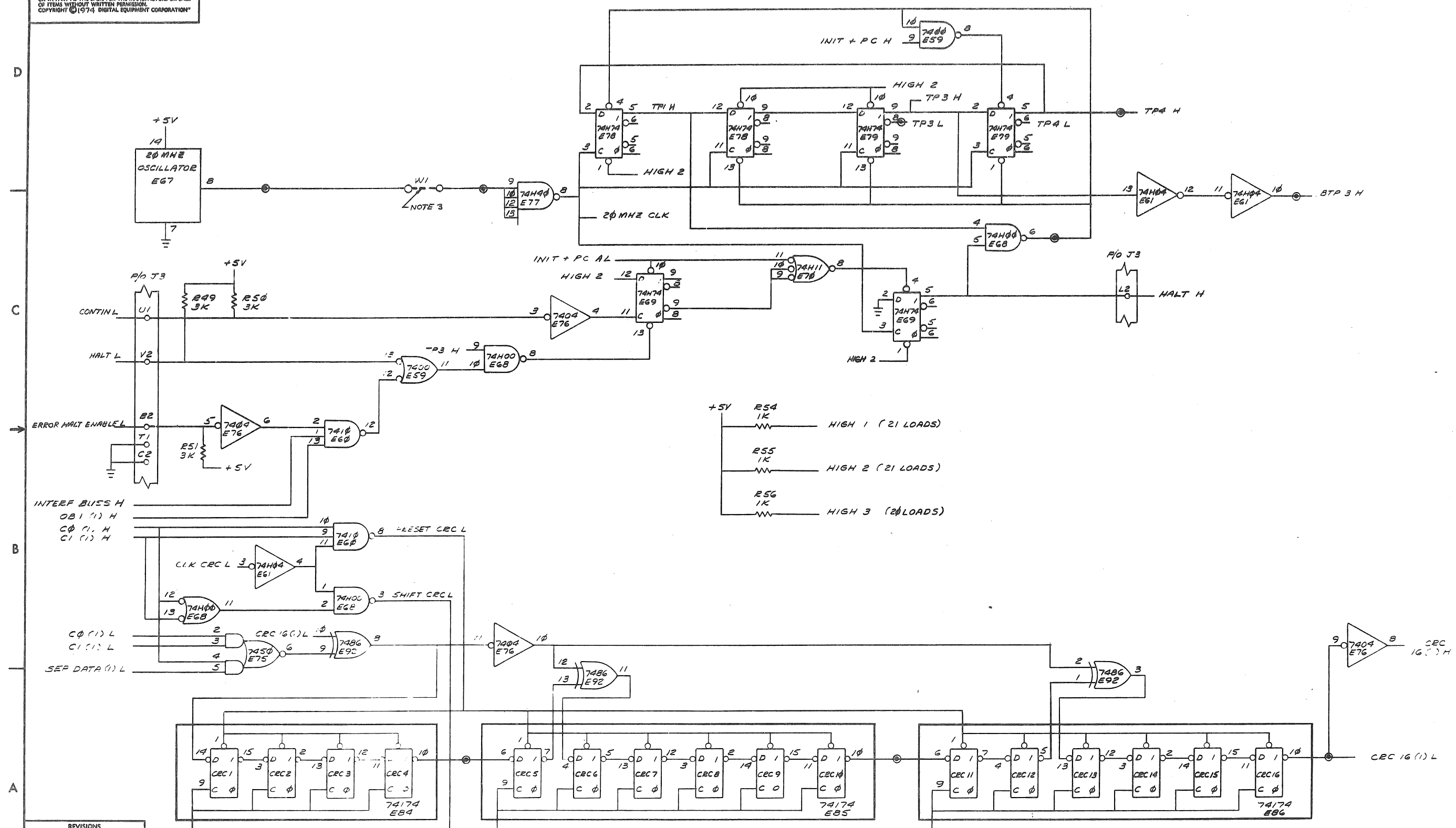


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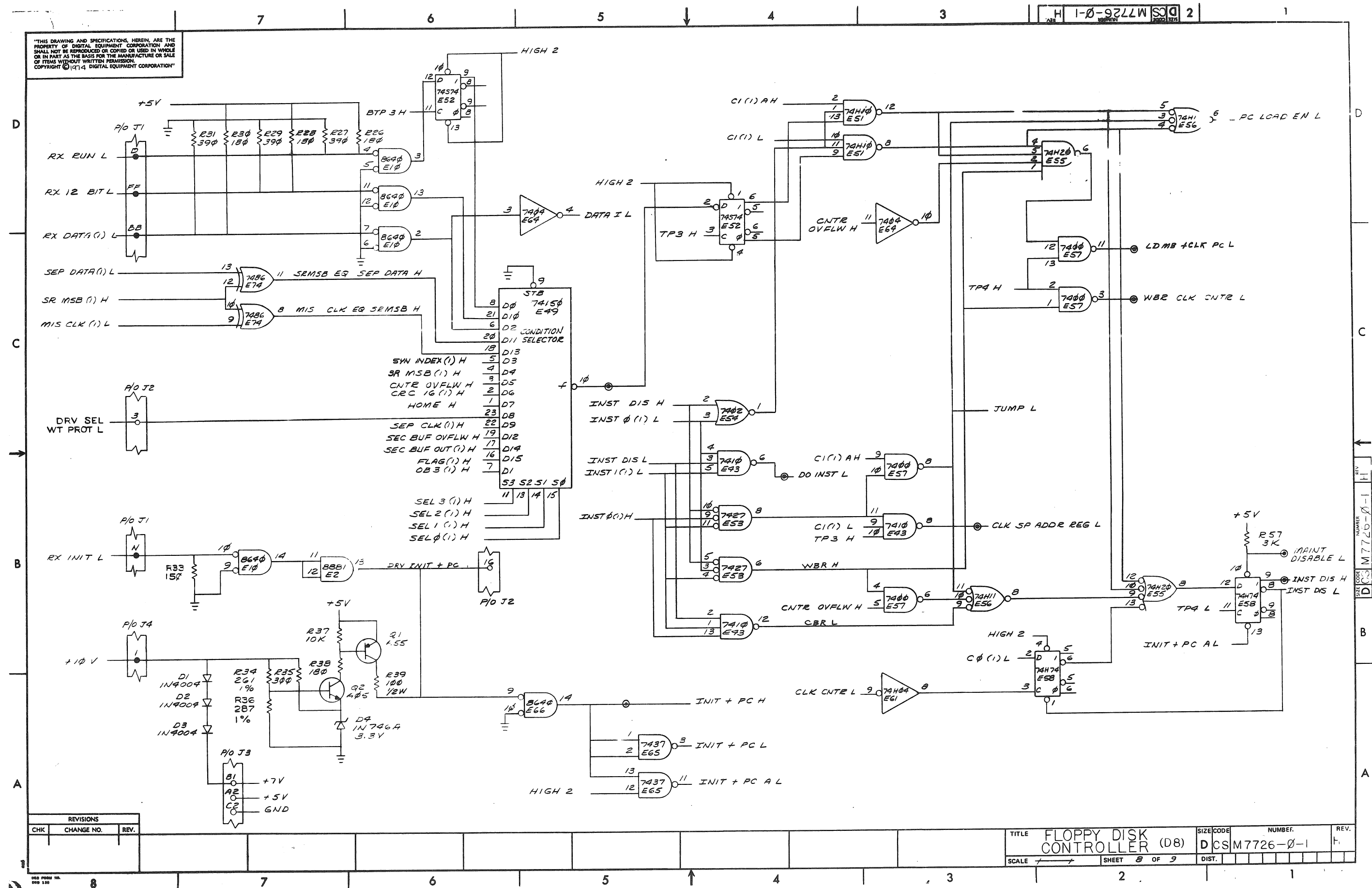
TITLE		FLOPPY DISK CONTROLLER (D5)		SIZE	CODE	NUMBER			REV.
				D	CS	M7726-0-1			H
SCALE		SHEET		OF		DIST.			
/ /		5		9					



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REVISIONS		
CHK	CHANGE NO.	REV.



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THIS LIST GIVES THE SOURCE AND DESTINATIONS OF SIGNAL NAMES WITHIN THE M7726 PRINT SET. SIGNAL NAMES THAT DO NOT APPEAR ON THIS LIST ARE PRESENT FOR INFORMATION ONLY. THEY DO NOT INDICATE CONNECTIONS TO OTHER POINTS IN THE PRINT SET.

INTERFACE REFERS TO SIGNALS ON THE INTERFACE BUSS
DRIVE REFERS TO SIGNALS ON THE DRIVE BUSS
POWER SUPPLY REFERS TO VOLTAGES FROM THE POWER SUPPLY
KM11 REFERS TO SIGNALS ON J3 THE MAINTENANCE CONNECTOR

SIGNAL NAME	ORIGIN	DESTINATION
BTP 3 H	D7-C1	D4-A5, D5-A6, D8-D6
CLK BAR L	D5-C7	D4-A3
CLK CNTR L	D5-B7	D3-B7, D8-A4
CLK CRC L	D5-C7	D7-B7
CNTR OVFLW H	D3-C5	D8-D4, D8-C6, D8-B4
CLK SFC BUF L	D5-C7	D4-B2
CLK SP ADDR REG L	D8-B3	D3-A4
CLK SR L	D5-H7	D3-B4
CONTIN L	KM11	D7-C7
CRC16 (1) H	D7-H1	D8-C6
CRC16 (1) L	D7-A1	D7-R7
C1 (1) AH	D3-A6	D4-R3, D5-B4, D8-D4, D8-C4
C1 (1) H	D3-A6	D3-C6, D3-B2, D7-B8
C1 (1) L	D3-A6	D5-D8, D7-R8, D8-D4, D8-B4
C0 (1) H	D3-A6	D3-C7, D3-A2, D4-B1, D5-B4, D7-R8
C0 (1) L	D3-A6	D3-R2, D4-B3, D7-R8, D8-B3
DATA 1 L	D8-D5	D4-A2
DISABLE ROMS L	TEST PAD	D6-D8
DD INST L	D8-H4	D5-H8
DRV BUSS H	D5-D4	D4-A4
DRV ERASE H	D5-B1	DRIVE
DRV OUT H	D5-C1	DRIVE
DRV LOAD HEAD H	D5-A1	DRIVE
DRV STEP L	D5-C1	DRIVE
DRV INIT + PC	D8-H6	UNLVE
DRV ABOVE TK 43 H	D5-H1	DRIVE
DRV RAW DATA L	UNLVE	D4-A8
DRV SEL CLK 1 H	D5-B1	DRIVE
DRV SEL INDX H	D5-A1	DRIVE
DRV SEL TRK 0 H	D5-B1	DRIVE
DRV WT DATA	D5-H1	DRIVE
DRV WT GATE H	D5-C1	DRIVE
DRV CEL WT PROT L	DRIVE	D8-C8
END WIND L	D4-D3	
ERROR HLT ENABLE L	KM11	D7-C7

FLAG (1) H	D5-B3	D8-B6
FLD 0 L	D6-D6	D6-A3, D6-A2
FLD 1 L	D6-D6	D6-B3, D6-B2
FLD 2 L	D6-D6	D6-C3, D6-C2
FLD 3 L	D6-D6	D6-A6, D6-A4
FLD 4 L	D6-D6	D6-B6, D6-B4
FLD 5 L	D6-D6	D6-C6, D6-C4
HALT H	D7-C3	KM11
HALT L	D7-C7	
HIGH 1	D7-C4	D3-D6, D3-D4, D3-C6, D3-C4, D4-A3
		D4-B1, D5-D5, D6-A8
HIGH 2	D7-B4	D4-A5, D5-B7, D5-A7, D5-B4, D7-D5
		D7-D4, D7-C4, D7-C5, D8-D5, D8-B3
		D8-A5
HIGH 3	D7-B4	D4-D8, D4-C8, D4-D7, D4-D5,
HOME H	D5-H2	D8-C6
INIT + PC A L	D8-A4	D3-C6, D3-B4, D3-A4, D3-A7, D4-B6
INIT + PC H	D8-A4	D4-B5, D6-B8, D7-C5, D8-B2
INIT + PC L	D8-A4	D4-D5, D4-C5, D7-D4
INST 0 (1) H	D3-B6	D4-R3, D5-R5, D6-A8
INST 0 (1) L	D3-H6	KM11, D8-R5
INST 1 (1) H	D3-B6	DR-C5
INST 1 (1) L	D3-B6	KM11
INST DIS H	D8-B1	DR-H5
INST DIS L	DR-R1	DR-C5
INTERF BUSS H	D5-D4	DR-H5
JUMP 1	DR-C3	D7-R8
		DR-C8
LD MR + CLK PC L	DR-C1	DR-AH, D3-AH
LD SCRATCH PAD L	D5-H6	D3-H1
MAINT DIS L	TEST PAD	D8-B1
MIS CLK (1) L	D4-C4	D8-C8
MUX OUT 0	D3-C7	D6-A8
MUX OUT 1	D3-C7	D6-A8
MUX OUT 2	D3-C7	D6-A8
MUX OUT 3	D3-C7	D6-B8
MUX OUT 4	D3-C7	D6-B8
MUX OUT 5	D3-D7	D6-H8
MUX OUT 6	D3-D7	D6-H8
MUX OUT 7	D3-D7	D6-B8

OB1 (1) H	D5-D4	D7-B8
OB3 (1) H	D5-C4	D8-B6
PC 0 (1) H	D6-A1	KM11
PC 1 (1) H	D6-A1	KM11
PC 2 (1) H	D6-A1	KM11
PC 3 (1) H	D6-A1	KM11
PC 4 (1) H	D6-A1	KM11
PC 5 (1) H	D6-A1	KM11
PC 6 (1) H	D6-A1	KM11
PC 7 (1) H	D6-A1	KM11
PC LOAD EN L	D8-D1	D6-A8
ROM OUT 0	D6-D1	D3-C8
ROM OUT 1	D6-D1	D3-C8
ROM OUT 2	D6-D1	D3-C8
ROM OUT 3	D6-D1	D3-C8
ROM OUT 4	D6-D1	D3-C8
ROM OUT 5	D6-D1	D3-D8
ROM OUT 6	D6-D1	D3-D8
ROM OUT 7	D6-D1	D3-D8
RX DATA (1) L	D5-C1, INTERFACE	INTERFACE, D8-D8
RX DONE L	D5-D1	INTERFACE
RX ERROR L	D5-D1	INTERFACE
RX INIT L	INTERFACE	DR-B8
RX OUT L	D5-D1	INTERFACE
RX RUN L	INTERFACE	D8-D8
RX SHIFT L	D5-C1	INTERFACE
RX TRANSFER REQUEST	D5-D1	INTERFACE
RX 12 HIT L	INTERFACE	D8-D8
SFC BUF OVFLW H	D4-A1	D8-C6
SFC BUF OUT (1) H	D4-C1	D5-C4, D8-B6
SFC BUF H	D5-H4	D5-C4
SEL 0 (1) H	D3-A6	D5-C8, D6-C8, D8-B6, KM11
SEL 1 (1) H	D3-A6	D5-C8, D6-C8, D8-B6, KM11
SEL 2 (1) H	D3-B6	D5-C8, D6-C8, D8-B6, KM11
SEL 3 (1) H	D3-B6	D5-C8, D6-C8, D8-B6, KM11
SEP CLK (1) H	D4-B4	D8-C6
SEP DATA (1) H	D4-R5	D3-A2
SEP DATA (1) L	D4-B5	D4-A2, D7-A8, D8-C8
SR H	D5-B4	D5-C4
SR LOAD H	D3-B1	D3-C4
SR MSB (1) H	D3-D3	D5-C4, D8-C8, D8-C6
SYN INDEX (1) H	D5-A5	D8-C6

TP3 H	D7-D3	D7-C6, D8-B4, D8-C5
TP3 L	D7-D3	D5-B8
TP4 H	D7-D2	D8-C3
TP4 L	D7-D3	D8-B2
WBR CLK CNTR L	D8-C2	D3-B7
20 MHZ CLK	D7-C5	D4-C8, D4-D7
GND	POWER SUPPLY	D1-A4
+5V	POWER SUPPLY	D1-A4, D8-A7
+7V	POWER SUPPLY	KM11
+10V	POWER SUPPLY	D8-B8

REVISIONS		
CHK	CHANGE NO.	REV.

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FIRST USED ON OPTION MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
RXØ1					
PARTS LIST					
DRN	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS TITLE FLOPPY CONTROLLER FIRMWARE			
CHK'D	DATE				
ENG	DATE				
PROJ. ENG.	DATE				
PROD.	DATE				
NEXT HIGHER ASSEMBLY					
SCALE		SIZE	CODE	NUMBER	REV.
SHEET 1 OF 1		K	SP	RXØ1-Ø-2	
		DIST.			

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/RX01 FLOPPY CONTROLLER FIRMWARE

/THIS SYMBOL TABLE REPLACES THE NORMAL PAL SYMBOL TABLE AND DEFINES
/THE INSTRUCTIONS POSSIBLE BY THE RX01 CONTROLLER

/DO INSTRUCTIONS

0002 SET=2
0000 CLR=0
0022 ONE=2
0000 ZERO=0

0000 IOB2=2
0004 IOB1=4
0012 IOB2=12
0014 IOB3=14
0020 IOB4=20
0024 IOB5=24
0030 IOB6=30

0000 INTERF=CLR IOB0
0002 DISK=SFT IOB0

0004 ERR=IOB1
0010 XREQ=IOB2
0014 IOOUT=IOB3
0020 DONE=IOB4
0024 SHIFT=IOB5
0030 SECDAT=IOB6

0004 MGATE=IOB1
0010 STPHD=IOB2
0014 HDOUT=IOB3
0020 EGATE=IOB4
0024 LOWCUR=IOB5

0034 UNIT=34

0040 UNHD=40
0042 LDHD=42

0044 BAR=44
0001 LONG=1
0000 SHORT=0
0002 INCR=2

/INTERFACE=DISK BUSS OUTPUT BUFFER

/IOB0 SELECTS EITHER INTERFACE OR DISK BUSS. CLR= INTERFACE
/SET=DISK

/INTERFACE BUFFER DEFINITIONS
/SET TO INDICATE THAT AN RX01 ERROR HAS OCCURED
/SET TO REQUEST AN RX01 WORD TRANSFER
/DIRECTION FOR DATA LINE. SET=TO INTERFACE
/SET TO INDICATE RX01 READYNES TO ACCEPT A COMMAND
/SHIFT FOR DATA LINE
/SELECTS SOURCE FOR DATA OUT OF CONTROLLER ON DATA LINE
/SET=SECTOR BUFFER CLR=SHIFT REGISTER MOST SIG BIT

/DISK BUFFER DEFINITIONS
/WRITE CURRET ENABLE WHEN SET
/HEAD STEP. TWO PULSES REQUIRED FOR EACH TRACK
/DIRECTION OF HEAD MOTION
/ERASE CURRENT ENABLE
/SPECIFIES WRITE CURRENT LEVEL

/SELECTS ONE OF TWO DRIVES. UNIT (ZERO)(ONE)

/DEACTIVATES HEAD LOAD SOLOINOID OF SELECTED DRIVE
/ACTIVATES HEAD LOAD SOLOINOID OF SELECTED DRIVE

/SECTOR BUFFER ADDRESS REGISTER CONTROL
/FORMAT: CLR BAR (SHORT)(LONG)
/SHORT PRESETS FOR COUNT OF 1024
/LONG PRESETS FOR COUNT OF 4096
/FORMAT: INCP BAR INCREMENT THE BUFFER ADDRESS REG.

/RX01 FLOPPY CONTROLLER FIRMWARE

PAL10

V142A 9-FEB-74

9:17

PAGE 1-1

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0050 WRTBUF=50
0003 START=3
0000 FINE=0

0054 CRC=54

0057 PRECRC=57
0055 DATCRC=55

0060 FLAG=60
0002 ON=2
0001 OFF=1
0003 TOG=3

0064 LSP=64

0070 LCT=70
0071 ESP=71
0073 ICT=73

0074 RCTATE=74

0075 LSR=75
0077 DATSR=77

/SECTOR BUFFER WRITE CLOCK
/FORMAT: (STPAT)(FIN) WRTBUF
/A 750NS MINIMUM PULSE IS REQUIRED

/CRC REGISTER CONTROL
/FORMAT: CRC (ONE)(ZERO) SPECIFIES DATA TO
/BE JAMMED INTO CRC GENERATOR/CHECKER
/PRESETS CRC REG TO ALL ONES
/SHIFTS SEPERATED DATA INTO CRC CIRCUIT

/GENERAL PURPOSE FLAG CONTROL
/FORMAT: FLAG (ON)(OFF)(TOG)
/SET FLAG
/CLR FLAG
/TOGGLE FLAG

/LOAD OPEN SCRATCHPAD REG WITH CONTENTS OF SHIFT REG
/LOAD COUNTER WITH CONTENTS OF NEXT ROM LOCATION
/LOAD COUNTER WITH CONTENTS OF OPEN SCRATCHPAD
/INCREMENT COUNTER

/SHIFT REGISTER CONTROL
/FORMAT: ROTATE(ONE)(ZERO)
/SHIFTS SHIFT REG TOWARDS MOST SIGNIFICANT BIT
/WHILE INSERTING A ONE OR ZERO INTO THE LEAST
/SIGNIFICANT BIT
/LOAD SHIFT REGISTER WITH CONTENTS OF COUNTER
/SHIFT REG TOWARDS MSB WHILE INSERTING SEPERATED
/DATA INTO LSR

/BRANCH INSTRUCTIONS AND CONDITIONS

0100	BR=100	/FORMAT: BR COND (T)(F)(ONE)(ZERO)
		/IF CONDITION IS MET, A BRANCH IS MADE WITHIN
		/THE CURRENT FIELD USING THE CONTENTS OF THE
		/NEXT ROM LOCATION AS THE BRANCH ADDRESS
		/IF THE CONDITION IS NOT MET, THE NEXT ROM LOCATION
		/IS IGNORED AND THE FOLLOWING INSTRUCTION IS EXECUTED
0300	WBR=300	/FORMAT: WBR COND (T)(ONE)
		/THE COUNTER IS INCREMENTED WITH EVERY EXECUTION OF
		/THIS INSTRUCTION. THE WBR IS REPEATEDLY
		/EXECUTED UNTILL EITHER THE COUNTER OVERFLOWS OR
		/THE CONDITION IS MET. IF THE CONDITION IS MET
		/THE BRANCH IS MADE. IF THE COUNTER OVERFLOWS
		/THE BRANCH ADDRESS IS IGNORED AND THE NEXT INSTRUCTION
		/IS EXECUTED
0000	F=ZERO	/REQUIRES THE CONDITION TO BE FALSE
0002	T=ONE	/REQUIRES THE CONDITION TO BE TRUE
0001	IND=1	/IF APPENDED TO THE JUMP, BR OR WBR INSTRUCTION,
		/CAUSES THE BRANCH ADDRESS TO BE TAKEN FROM THE
		/OPEN SCRATCHPAD RATHER THAN FROM THE NEXT ROM LOCATION
0000	PUN=0	/WHEN ASSERTED INDICATES THAT THE INTERFACE HAS
		/SERVICED A TRANSFER REQUEST, OR THAT A COMMAND
		/IS PENDING
0004	IOB30T=4	/INTERF/DISK OUTPUT BUFFER BIT 3
0010	DATAIN=10	/BIDIRECTIONAL DATA LINE BETWEEN INTERFACE AND CONTROLLER
0014	INDX=14	/DRIVE INDEX LATCH
0020	SR7=20	/SHIFT REGISTER MOST SIGNIFICANT BIT
0024	COFL=24	/OVERFLOW (ALL ONES) OF THE COUNTER
0030	CRC16=30	/BIT 16 OF CRC GENERATOR/CHECKER
0034	HOME=34	/TRACK ZERO OF SELECTED DRIVE AND ED WITH HEAD
		/DIRECTION BEING OUT
0040	WRTEN=40	/WRITE ENABLED STATUS OF THE SELECTED DRIVE
0044	SEPCLK=44	/SEPERATED CLOCK FROM DISK DATA
0050	XIIBIT=50	/ASSERTED IF INTERFACE TRANSFERS ARE TO BE AS
		/12 BIT WORDS RATHER THAN 8 BIT BYTES
0054	DEQSR7=54	/SEPERATED DATA EQUAL TO SHIFT REG BIT 7
0060	BAROFL=60	/OVERFLOW CONDITION (ALL ONES) OF THE SECTOR BUFFER
		/ADDRESS REGISTER
0064	MCEQSR=64	/MISSING CLOCK EQUAL TO SHIFT REG BIT 7
0070	BOATAO=70	/OUTPUT OF SECTOR BUFFER
0074	FLAGO=74	/STATE OF GENERAL PURPOSE FLAG

/SCRATCHPAD REGISTER SELECTION

0200	OPEN=200	/FORMAT: OPEN X WHERE X IS ONE OF THE SCRATCHPAD REG
		/THIS INSTRUCTION MAKES THE NAMED SCRATCHPAD
		/ACCESSABLE VIA THE LSP AND ESP COMMANDS

/DEFINITIONS OF SCRATCHPADS BY R#

0000	R#00
0004	R1=4
0010	R2=10
0014	R3=14
0020	R4=20
0024	R5=24
0030	R6=30
0034	R7=34
0040	R8=40
0044	R9=44
0050	R10=50
0054	R11=54
0060	R12=60
0064	R13=64
0070	R14=70
0074	R15=74

/DEFINITION OF SCRATCHPADS BY PNEUMONICS

0000	CURTKO=R0	/CURRENT TRACK ADDRESS OF DRIVE 0
0004	CURTK1=R1	/CURRENT TRACK ADDRESS OF DRIVE 1
0010	ERREG=R2	/DEFINITIVE ERROR CODE IF ANY
0014	STAT=R3	/STATUS WORD OF RX01
0020	TARTRK=R4	/TARGET TRACK OF CURRENT DISK ACCESS
0024	TARSEC=R5	/TARGET SECTOR OF CURRENT DISK ACCESS
0030	TEMPA=R6	/TEMPORARY STORAGE
0034	TEMPB=R7	/TEMPORARY STORAGE
0040	TEMPC=R8	/TEMPORARY STORAGE
0044	TEMPE=R9	/TEMPORARY STORAGE
0050	TEMPF=R10	/BIT 7 IS UNIT SELECT BIT. 0 MEANS UNIT 1
0054	TEMPG=R11	/BIT 7 IS HEAD LOADED BIT. 1 MEANS HEAD LOADED
0060	TEMPE=R12	/TEMPORARY STORAGE
0064	RTNR=R13	/RETURN ADDRESS FOR 3RD LEVEL NESTED SUBROUTINES
0070	RTNA=R14	/RETURN ADDRESS FOR 2ND LEVEL NESTED SUBROUTINES
0074	PTNR=R15	/RETURN ADDRESS FOR 1ST LEVEL SUBROUTINES

/JUMP INSTRUCTION AND JUMP FIELD DEFINITIONS

2272 JUMP=222 /FORMAT: JUMP EX (IND)
/CAUSES A BRANCH TO ONE OF SIX ROM FIELDS (0-5)
/SPECIFIED BY X. THE BRANCH ADDRESS IS TAKEN FROM
/THE ROM LOCATION FOLLOWING THE JUMP INSTRUCTION.
/IF IND IS APPENDED, THE BRANCH ADDRESS
/IS TAKEN FROM THE OPEN SCRATCH PAD

2202 F0=0
2204 F1=0
2206 F2=12
2210 F3=14
2214 F4=20
2220 F5=24

/TABLE OF DEFINITIVE ERROR CODES

0010	KXDOV0=10	/DRIVE 0 FAILED TO SEE HOME ON INITIALIZE	
0020	KXDOV1=20	/DRIVE 1 FAILED TO SEE HOME ON INITIALIZE. DOES NOT CAUSE ERROR	
0030	KARONG=30	/FOUND HOME WHEN STEPPING IN 10 TRACKS FOR INIT	
0040	KERTRK=40	/TRIED TO ACCESS A TRACK GREATER THAN 76	
0050	KHOMERR=50	/HOME WAS FOUND BEFORE DESIRED TRACK WAS REACHED	
0060	KSELFERR=60	/SELF DIAGNOSTIC ERR	
0070	KXHDR=70	/DESIRED SECTOR COULD NOT BE FOUND AFTER LOOKING	
		/AT 52 HEADERS	
0100	KAPROT=100	/WRITE FUNCTION ATTEMPTED ON A WRITE PROTECTED DISK	
0110	KTIMER=110	/MORE THAN 40 MCHSECONDS AND NO SEPCLOCK SEEN	
0120	KXPRAM=120	/A PREAMBLE COULD NOT BE FOUND	
0130	KXIDAM=130	/PREAMBLE FOUND BUT NO ID MARK FOUND WITHIN ALLOWABLE TIME	
0140	KHCRCER=140	/CRC ERROR ON WHAT APPEARED TO BE A HEADER. ERROR IS NOT ASSERTED	
0150	KTKSKER=150	/THE TRACK ADDRESS OF A GOOD HEADER DOES NOT COMPARE	
		/WITH THE DESIRED TRACK	
0160	KXSTRYS=160	/TOO MANY TRIES FOR AN IDAM	
0170	KNOGAM=170	/DATA AM NOT FOUND IN ALLOTTED TIME	
0200	KDCRCER=200	/CRC ERROR ON READING THE SECTOR FROM THE DISK	
0210	KPARER=210	/PARITY ERROR ON SOME WORD FROM THE INTERFACE	

220 /ROUTINE: INITIALIZE/ IF A HOST PROCESSOR INITIALIZE OR AN
 221 /RX01 POWER LOW IS DETECTED, THE PC IS CLEARED AND THE RX01 TIMING
 222 /STOPS. UPON THE NEGATION OF INITIALIZE, TIMING RESUMES AND A SELF TEST OF
 223 /INTERNAL DATA PATHS IS MADE. IF AN ERROR OCCURS HERE, ERROR AND
 224 /DONE ARE SET, BUT ERREG IS NOT ALTERED. THEN IF NO ERROR HAS OCCURRED AN ATTEMPT
 225 /IS MADE TO RECALIBRATE DRIVE 1 THEN DRIVE 0. IF DRIVE 0 FAILS TO RECALIBRATE,
 226 /THE ERROR CODE IS LOADED INTO ERREG AND ERROR IS SET. IF DRIVE
 227 /RECALIBRATES AND IS READY (DISK LOADED) SECTOR ONE OF TRACK ONE
 228 /IS READ INTO THE SECTOR BUFFER. IT IS POSSIBLE FOR A READ ERROR
 229 /TO OCCUR WHILE READING THIS SECTOR.

230	0000	*2700	DECIMAL	
231				
232				
233				
234	0000	0210	OPEN ERREG	/CLEAN ERROR REGISTER
235	0001	0064	LSP	
236				
237	0022	0222	JUMP F4	/GO DO THE INITIALIZE DIAGNOSTIC ROUTINE
238	0033	2352	TEST	
239				
240	0004	0070	TSTRN, LCT	/RETURN FROM SUCCESSFUL DIAGNOSTIC ROUTINE
241			OCTAL	
242	0005	0024	"	
243				
244	0006	0075	DECIMAL	
245	0007	0014	LSR	/SET THE INIT DONE BIT OF STAT
246	0010	0064	OPEN STAT	
247			LSP	
248	0011	0070	LCT	/SET UP SOME 3CPATCHPAD REGISTERS
249	0012	0377	-1	
250	0013	0075	LSR	
251	0014	0204	OPEN TEMPD	/UNIT 0 TO SOFT UNIT BIT
252	0015	0064	LSP	
253	0016	0200	OPEN CURTK0	/NEG ZERO TO BOTH CURRENT TRACK ADDRESSES
254	0017	0064	LSP	
255	0020	0204	OPEN CURTK1	
256	0021	0064	LSP	
257				
258	0022	0074	ROTATE ZERO	/NEG ONE TO TARGET SECTOR
259	0023	0224	OPEN TARSEC	
260	0024	0064	LSP	
261	0025	0220	OPEN TARTRK	/NEG ONE TO TARGET TRACK FOR INITIALIZE BOOTSTRAP
262	0026	0064	LSP	
263				
264	0027	0002	DISK	/SELECT DISK RUSS
265				
266	0030	0070	LCT	
267	0031	0034	RECALL1	/CALL SUBROUTINE TO LOAD HEAD AND WAIT 25 MS
268	0032	0222	JUMP F4	/TO ALLOW POWER UP DRIVE SETTLE TIME
269	0033	2145	DLY25	
270				
271	0034	0036	RECALL1, UNIT ONE	/SELECT UNIT ONE FOR RECALIBRATE
272				
273	0035	0014	RECALL0, CLR HDOUT	/STEP HEAD IN 1" TRACKS TO ASSURE IT IS NOT BEHIND TRACK 0
274				

275	0036	0070	LCT	
276	0037	0305	-10-1	
277	0040	0075	LSR	
278	0041	0070	LCT	
279	0042	0045	INIT	
280	0043	0222	JUMP F4	
281	0044	2100	STEPHD	
282				
283	0045	0220	JUMP F5	/ERROR. HOME WAS SEEN WHILE STEPPING IN.
284	0046	2621	WRONG	
285				
286	0047	0010	SET HDOUT	/STEP OUT AS MANY AS 80 TRACKS IN SEARCH OF HOME
287	0050	0070	LCT	
288	0051	0257	-80-1	
289	0052	0075	LSR	
290	0053	0070	LCT	
291	0054	0060	RCALOK	
292	0055	0040	UNHD	
293	0056	0222	JUMP F4	
294	0057	2100	STEPHD	
295				
296	0060	0202	RCALOK, JUMP F0	/HOME WAS FOUND OK
297	0061	0075	WHCHDR	
298				
299	0062	0174	BR FLAGO F	/IF FLAG=0 RECALIBRATE WAS ON DRIVE 1
300	0063	0070	NXDRV1	
301				
302	0064	0070	LCT	/RECALIBRATE FAILURE WAS ON DRV 0
303	0065	0010	KNXDV0	
304	0066	0226	JUMP F5	
305	0067	2610	GOERDN	
306				
307	0070	0070	LCT	/RECAL FAILURE WAS ON DRV 1, LOG ERROR
308	0071	0020	KNXDV1	/AND CONTINUE RECALIBRATION
309	0072	0075	LSR	
310	0073	0210	OPEN ERREG	
311	0074	0064	LSP	
312				
313	0075	0176	WHCHDR, BR FLAGO T	/IF FLAG=1 BOTH DRIVES HAVE BEEN RECALIBRATED
314	0076	0372	PUNRCL	
315				
316	0077	0062	FLAG ON	/SET FLAG TO INDICATE DRV 0 IS BEING RECALIBRATED
317				
318	0100	0034	UNIT ZERO	
319				
320	0101	0202	JUMP F0	/GO BACK AND RECALIBRATE DRV0
321	0102	0035	RECAL0	

322 /SUBROUTINE: FINDTRACK]
323 /THIS SUBROUTINE IS USED TO LOCATE A SPECIFIED SECTOR. IT PICKS
324 /UP THE TRACK AND SECTOR ADDRESS FROM THE INTERFACE, CHECKS THAT
325 /THE TRACK ADDRESS IS LEGAL (NOT GREATER THAN 114 OCTAL.), MOVES THE
326 /HEAD OF THE SELECTED DRIVE TO THE SPECIFIED TRACK, VERIFIES
327 /TRACK POSITION, AND LOCATES THE CORRECT SECTOR. EXIT FROM
328 /THIS SUBROUTINE OCCURS AT PRITE TURN ON TIME OF THE SELECTED.
329 /SECTOR. ENTRANCE IS MADE WITH THE RETURN ADDRESS IN THE COUNTER
330

331	0103 0075	FINDTR, LSR	/SAVE THE RETIR" ADDRESS
332	0104 0274	OPEN RTN	
333	0105 0064	LSP	
334	0106 0270	LCT	/CLEAR THE ERROR REGISTER
335	0107 0000	V	
336	0110 0075	LSR	
337	0111 0212	OPER. ERPEG	
338	0112 0064	LSP	
339	0113 0244	OPER TEMPD	/SOFT UNIT BIT TO SR
340	0114 0071	ESP	
341	0115 0075	LSR	
342	0116 0122	BR SR7 ONE	/IF SR=1 DRIVE 0 IS CURRENTLY SELECTED
343	0117 0127	UZERO	
344	0120 0174	UONE,	/IF FLAG=0 DRIVE 1 IS DESIRED AND ALREADY SELECTED
345	0121 0101	USAME	
346	0122 0034	UNIT ZERO	/DRIVE 0 IS DESTRED AND DRIVE1 WAS SELECTED, SELECT 0
347	0123 0070	LCT	/SET UP SOFT UNIT SELECT AS DRIVE 0
348	0124 0204	OCTAL	
349	0125 0202	200	
350	0126 0134	DECIMAL	/GO STORE SOFT UNIT BIT
351	0127 0176	JUMP F4	
352	0130 0141	UDIF	/IF FLAG=1 DRIVE 0 IS DESIRED AND ALREADY SELECTED
353	0131 0036	UNIT ONE	
354	0132 0070	LCT	/DRIVE 1 IS DESTRED BUT DRIVE0 IS SELECTED, SELECT DRIVE 1
355	0133 0004	0	/SET UP SOFT UNIT SELECT BIT AS DRIVE 1
356	0134 0075	LSR	/STORE SOFT UNIT SELECT BIT
357	0135 0064	LSP	
358	0136 0074	ROTATE ZERO	/CLK SOFT HD LOAD BIT BECAUSE UNITS CHANGED
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377 OPEN TEMPE

LSP

378 0140 0064

USAME,

LCT

/CALL GETWORD SUBROUTINE FOR THE SECTOR ADDRESS

379 0141 0070

PUTSEC

JUMP F4

GETWRD

380 0142 0145

PUTSEC

JUMP F4

GETWRD

381 0143 0222

382 0143 0222

383 0144 2000

384 0145 0070

PUTSEC,

LCT

-77=1

ROTATE ONE

BR COFL T

387 0147 0076

388 0150 0126

389 0151 0160

390 0152 0073

391 0153 0122

392 0154 0147

393 0155 0074

394 0156 0202

395 0157 0150

396 0160 0224

397 0161 0064

398 0162 0070

399 0163 0166

400 0164 0222

401 0165 2000

402 0166 0220

403 0167 0064

404 0170 0254

405 0171 0064

406 0172 0260

407 0173 0070

408 0174 0262

409 0175 0075

410 0176 0064

411 0177 0070

412 0200 0206

413 0201 0075

414 0202 0270

415 0203 0064

416 0204 0226

417 0205 2400

418 0206 0202

419 0207 0242

420 0210 0202

421 0211 0242

422 0211 0242

423 0211 0242

424 0211 0242

425 0211 0242

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585 0211 0242

586 0211 0242

587 0211 0242

588 0211 0242

589 0211 024

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/RX01 FLOPPY CONTROLLER FIRMWARE          PAL12          9:17      PAGE 7-2
VI42A  9-FEB-74

0212 0244      OPEN TEMPO
0213 0071      ESP
0214 0075      LSR

0215 0200      OPEN CURTK0
0216 0002      DISK

0217 0122      BR SR7 ONE
0220 0222      *+2
0221 0204      OPEN CURTK1

0222 0071      ESP
0223 0075      LSR
0224 0200      OPEN TEMPG
0225 0064      LSP

0226 0220      OPEN TARTRK
0227 0071      ESP
0230 0075      LSR
0231 0254      OPEN TEMPF
0232 0064      LSP
0233 0070      LCT
0234 0246      TRKEG
0235 0075      LSP
0236 0270      OPEN RTNA
0237 0064      LSP
0240 0226      JUMP F5
0241 2403      MAGCOM

0242 0070      ERTEK, LCT
0243 0040      KERTRK
0244 0226      JUMP F5
0245 2610      GUERDN

0246 0202      TRKEG, JUMP F0
0247 0357      NUSTPS
0250 0270      OPEN RTNA
0251 0270      OPEN RTNA

0252 0270      BOOT, OPEN RTNA
0253 0070      LCT
0254 0275      STPOUT
0255 0075      LSR
0256 0064      LSP

0257 0244      OPEN TEMPO
0260 0071      ESP
0261 0075      LSR

0262 0204      OPEN CURTK1
0263 0120      BR SR7 ZERO

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/RX01 FLOPPY CONTROLLER FIRMWARE          PAL10          9:17      PAGE 7-3
VI42A  9-FEB-76

0264 0266      *+2
0265 0200      OPEN CURTK0

0266 0071      ESP
0267 0075      LSR

0270 0220      OPEN TARTRK
0271 0071      ESP

0272 0016      SET HDOUT

0273 0226      JUMP F5
0274 2462      DIF

0275 0202      STPOUT, JUMP F0
0276 0300      *+2

0277 0014      CLR HDOUT

0300 0070      LCT
0301 0305      DUNSTP

0302 0040      UNHD

0303 0222      JUMP F4
0304 2100      STEPHD

0305 0226      DUNSTP, JUMP F5
0306 2456      HOMERR

0307 0244      OPEN TEMPD
0310 0071      ESP
0311 0075      LSR
0312 0220      OPEN TARTRK
0313 0071      ESP

0314 0200      OPEN CURTK2
0315 0122      BR SR7 ONE
0316 0320      *+2
0317 0204      OPEN CURTK1

0320 0075      LSR
0321 0064      LSP

0322 0220      HDSETL, OPEN TARTRK
0323 0071      ESP
0324 0075      LSR
0325 0254      OPEN TEMPF
0326 0064      LSP

0327 0070      LCT
0330 0323      -40-1

```

VI42A 9-FEB-74 9:17 PAGE 7-2

/TARGET TRACK IS OK, GET THE DRIVE
/SELECT FROM TEMPO

/PRESELECT UNIT 0

/SELECT DISK BUS

/WHICH UNIT SELECTED? BIT7=0 MEANS UNIT ONE
/ZERO, SKIP UNIT 1 SETUP

/PASS SELECTED CURRENT TRACK TO MAGCOM SUBR

/PASS TARGET TRACK TO MAGCOM SUBROUTINE

/CALL SUBROUTINE MAGCOM TO SEE IF TARGET
/IS SAME AS CURRENT TRACK. F=TARGET, G=CURRENT

/TRIED TO ACCESS A TRACK GREATER THAN 76 DECIMAL

/TARGET EQUALS THE CURRENT TRACK, NO
/STEPS ARE REQUIRED
/NOOP; TARGET > ACTUAL RETURN
/NOOP

/TARGET IS LESS THAN ACTUAL, STEPS NEEDED ALSO START OF
/OF BOOT SUBROUTINE. SET UP RETURN FROM DIF SUBR

/SOFT UNIT SELECT BIT TO SR7

/PRESELECT UNIT 1

/SR7=0 MEANS UNIT ONE

VI42A 9-FEB-76 9:17 PAGE 7-3

/PASS SELECTED CURRENT TRACK TO DIF SUBR VIA SR

/PASS TARGET TRACK TO DIF VIA CNTR

/ASSUME A STEP OUT

/GO TO THE SUBROUTINE DIF TO CALCULATE THE STEPS NEEDED

/TARGET TRACK IS LESS THAN
/THE ACTUAL, MOVE OUT IS NECESSARY

/TARGET IS GREATER THAN ACTUAL. STEPS IN NEEDED

/COMPLEMENT OF STEPS REQUIRED IS IN THE
/SHIFT REG. SET UP RETURN FROM STEPHD SUBR

/UNLOAD HEAD BEFORE MOVING

/CALL SUBROUTINE STEPHD

/HOME FOUND BEFORE LAST STEP TAKEN

/SOFT UNIT BIT TO SR7

/GET READY TO PASS TARGET TRK TO PROPER
/CURRENT TRACK

/OPEN PROPER CURRENT TRACK REGISTER
/BIT7=0 MEANS UNIT ONE

/UPDATE THE CURRENT TRACK ADDRESS

/HEAD IS SETTLED, DETERMINE IF ABOVE TRACK 43 DECIMAL
/PASS TARGET TO MAGCOM VIA TEMPF

/PASS 44 TO MAGCOM VIA TEMPG

```
502 0331 0075 LSR
503 0332 0260 OPEN TEMP
504 0333 0064 LSP
505
506 0334 0026 /ASSUME TARGET GREATER THAN 43
507
508 0335 0070 LCT
509 0336 0344 ARV43
510 0337 0075 LSR
511 0340 0270 OPEN RTNA
512 0341 0064 LSP
513 0342 0226 JUMP F5
514 0343 2400 /AGCOM
515
516 0344 0202 ARV43, JUMP F0
517 0345 0346 .+1
518
519 0346 0202 JUMP F0
520 0347 0351 .+2
521
522 0350 0024 CLR LOWCUR
523
524 0351 0070 CFIRSE, LCT
525 0352 0355 RFINTR
526 0353 0206 JUMP F1
527 0354 0714 FINDERSE
528
529 0355 0274 RFINTR, OPEN RTN
530 0356 0207 JUMP F1 IND
531
532
533 0357 0250 HOSTPS, OPEN TEMPE
534 0360 0071 ESP
535 0361 0075 LSR
536
537 0362 0122 BR SR7 ONE
538 0363 0322 HDSETL
539
540 0364 0070 LCT
541 0365 0322 HDSETL
542 0366 0222 JUMP F4
543 0367 2145 DLY25
544
545
546 0370 0212 PFUNCT, JUMP F2
547 0371 1036 FUNCT
548
549 0372 0226 PDHREL, JUMP F5
550 0373 2625 DNRCL
551
552 0374 0000 0
553 0375 0000 3
554 0376 0000 0
555 0377 0000 0
556
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/ROUTINE: WRITE SECTOR]
/THIS ROUTINE TURNS ON WRITE GATE AT WRITE TURN ON TIME,
/Writes a preamble of 6 bytes of zeroes, a data or deleted data mark,
/then turns on erase gate. enter with CNTR=100 if
/deleted data, CNTR=0 if normal data mark. the data mark, data field, CRC
/and one byte postamble are written. write current is turned off.
/511 micro seconds later erase current is turned off. a header must
/then be read to insure disk is still up to speed before the write
/sector function is complete.

0400 0214 WRTSEC, OPEN STAT
0401 0075 LSR
0402 0064 LSP
0403 0070 LCT
0404 0407 S*GATE
0405 0202 JUMP F0
0406 0103 FINDERP
0407 2061 S*GATE, FLAG OFF
0408 0140 BR WRTEN F
0409 0503 PRTERP
0410 0214 OPEN STAT
0411 0071 ESP
0412 0406 SET W*GATE
0413 0075 LSR
0414 0074 ROTATE ZERO
0415 0234 OPEN TEMPB
0416 0057 PRECRC
0417 0056 CRC ONE
0418 0056 CRC ONE
0419 0056 CRC ONE
0420 0056 CRC ONE
0421 0054 CRC ZERO
0422 0120 BR SR7 ZERO
0423 0460 DAMSUP
0424 0070 LCT
0425 0325 OCTAL
0426 0325 DECIMAL
0427 0054 CRC ZERO
0428 0054 CRC ZERO
0429 0002 DISK
0430 0002 DISK
0431 0070 LCT
0432 0325 OCTAL
0433 0054 CRC ZERO
0434 0054 CRC ZERO
0435 0002 DISK
0436 0002 DISK
0437 0054 CRC ZERO
0438 0054 CRC ZERO
0439 0002 DISK
0440 0002 DISK
0441 0054 CRC ZERO
0442 0054 CRC ZERO
0443 0002 DISK
0444 0002 DISK
0445 0054 CRC ZERO
0446 0054 CRC ZERO
0447 0002 DISK
0448 0002 DISK
0449 0054 CRC ZERO
0450 0054 CRC ZERO
0451 0002 DISK
0452 0002 DISK
0453 0054 CRC ZERO
0454 0054 CRC ZERO
0455 0002 DISK
0456 0002 DISK
0457 0054 CRC ZERO
0458 0054 CRC ZERO
0459 0002 DISK
0460 0002 DISK
0461 0054 CRC ZERO
0462 0054 CRC ZERO
0463 0002 DISK
0464 0002 DISK
0465 0054 CRC ZERO
0466 0054 CRC ZERO
0467 0002 DISK
0468 0002 DISK
0469 0054 CRC ZERO
0470 0054 CRC ZERO
0471 0002 DISK
0472 0002 DISK
0473 0054 CRC ZERO
0474 0054 CRC ZERO
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0490 0054 CRC ZERO
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0493 0054 CRC ZERO
0494 0054 CRC ZERO
0495 0002 DISK
0496 0002 DISK
0497 0054 CRC ZERO
0498 0054 CRC ZERO
0499 0002 DISK
0500 0002 DISK
0501 0054 CRC ZERO
0502 0054 CRC ZERO
0503 0002 DISK
0504 0002 DISK
0505 0054 CRC ZERO
0506 0054 CRC ZERO
0507 0002 DISK
0508 0002 DISK
0509 0054 CRC ZERO
0510 0054 CRC ZERO
0511 0002 DISK
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0514 0054 CRC ZERO
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0516 0002 DISK
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0605 0054 CRC ZERO
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0641 0054 CRC ZERO
0642 0054 CRC ZERO
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0996 0002 DISK
0997 0054 CRC ZERO
0998 0054 CRC ZERO
0999 0002 DISK
1000 0002 DISK
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652	0437 0063	STASH,	TOG FLAG	/END OF THE FIRST 0 BIT
653			LSR	/PUT SECOND HALF OF THE DESIRED MARK IN THE TEMPB
654	0440 0075		LSP	
655	0441 0064			/SET UP RETURN FROM WRITE ZEROS SUBROUTINE
656			LCT	
657	0442 0070		HLFCLY	
658	0443 0466		LSR	
659	0444 0075			/STALL 1.8 MICRO SECONDS
660			LCT	
661	0445 0070		-3-1	
662	0446 0374		ICT	
663	0447 0073		BR COFL F	
664	0450 0124		-2	
665	0451 0447		DISK	/NOOP
666	0452 0002			
667			LCT	/SPECIFY 22 ZEROS TO BE WRITTEN BY WRT0S SUBROUTINE
668	0453 0070		-22-1	
669	0454 0351			
670			TOG FLAG	/WRITE SECOND CLOCK TRANSITION
671	0455 0063		JUMP F2	/CALL WRITE ZEROS SUBROUTINE
672	0456 0212		WRT0S	
673	0457 1322			/LOAD SECOND HALF OF NORMAL DATA MARK
674		DANSUP,	LCT	
675	0460 0070		OCTAL	
676			337	
677	0461 0337		DECIMAL	
678			CRC ONE	/JAN LAST 2 BITS OF DATA MARK TO CRC GENERATOR
679	0462 0056		CRC ONE	
680	0463 0056			/GO PUT AWAY THE SECOND HALF OF THE DATA MARK
681	0464 0200		JUMP F1	
682	0465 0437		STASH	/NOOP
683			HLFCLY, DISK	
684	0466 0002			/SET UP RETURN FROM WRITE ZEROS SUBROUTINE
685			LCT	
686	0467 0070		WRTDAM	
687	0470 0514		LSR	
688	0471 0075			/NOOP WASTE .P MICRO SECONDS
689			LCT	/NOOP
690	0472 0070		-22-1	/NOOP
691	0473 0351		LCT	
692	0474 0070		-22-1	/SPECIFY 22 BITS TO BE WRITTEN BY WRT0S SUBROUTINE
693	0475 0351			
694			LCT	
695	0476 0070		-22-1	/WRITE THE 25TH CLOCK TRANSITION
696	0477 0351			/CALL WRT0S SUBROUTINE
697			TOG FLAG	
698	0500 0063		JUMP F2	
699	0501 0212		WRT0S	
700	0502 1322			
701				
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761				

707	0503 0070	PRERR, LCT		/SET WRITE PROTECT BIT OF STAT BECAUSE A WRITE FUNCTION WAS ATTEMPTED ON
708				/ON A WRITE PROTECTED DISKETTE
709				
710	0504 0010		OCTAL	
711			10	
712	0505 0075		DECIMAL	
713	0506 0214		LSR	
714	0507 0064		OPEN STAT	
715			LSP	
716	0510 0070		LCT	/ERROR CODE FOR WRT PROTECT ERROR
717	0511 0100		KMPROT	
718	0512 0226		JUMP F5	
719	0513 2610		GOERDN	
720				
721				
722				
723				
724				
725				
726				
727				
728				
729	0514 0070	WRTDAM, LCT		
730	0515 0375		-2-1	/WASTE 2.0 MICRO SECONDS
731	0516 0073		ICT	
732	0517 0075		LSR	
733	0520 0124		BR COFL F	
734	0521 0516		-3	
735			TOG FLAG	
736	0522 0063			/WRITE A CLOCK BIT AS END OF 48TH ZERO
737			LCT	/FIRST HALF OF DATA MARK PATTERN TO SR
738	0523 0070		OCTAL	
739	0524 0352		352	
740			DECIMAL	
741	0525 0075		LSR	
742				/SET TRANSITION LOOP COUNTER FOR 8 LOOPS
743	0526 0070		LCT	
744	0527 0370		-7-1	/NOOP
745	0530 0002		DISK	
746				/WHATS THE BIT?
747	0531 0120	AGAIN, A	BR SR7 ZERO	/ZERO, NO TRANSITION
748	0532 0562			/ONE, RESET THE BUFFER ADDR REG TO 0
749			CLR BAR	/WRITE FLUX TRANSITION
750	0533 0044		TOG FLAG	/CHECK TRANSITION LOOP COUNT
751				/GO GET SECOND HALF
752	0534 0063			/SHIFT NEXT TRANSITION TO SR7
753	0535 0126	ABACK, A	BR COFL T	/BUMP TRANSITION LOOP COUNTER
754	0536 0543		SECHLF	
755				
756				
757	0537 0074		ROTATE	
758				
759				
760	0540 0073		ICT	
761				

762	0541 0206	JUMP F1	/DO ANOTHER LOOP
763	0542 0531	AGAIN	
764			
765	0543 0234	SECHLF, OPEN TEMP8	/SECOND HALF OF DATA MARK TO SR
766	0544 0071	ESP	
767	0545 0075	LGR	
768			/SET TRANSITION LOOP COUNTER FOR 8 LOOPS
769	0546 0070	LCT	
770	0547 0370	-7-1	
771			
772			
773	0550 0120	AGAIN1, BR SR7 ZERO	/SHALL WE WRITE A TRANSITION?
774	0551 0564	B	/NO
775			
776	0552 0263	TOG FLAG	/YES
777	0553 0002	DISK	/NOOP
778			
779	0554 0126	BACK, BR COFL T	/DONE DATA MARK?
780	0555 0566	WRTDAT	/YES, GO WRITE DATA
781			
782	0556 0073	ICT	/NO, BUMP THE LOOP COUNTER
783			
784	0557 0074	ROTATE	/BRING UP NEXT HALF BIT TO SR7
785			
786	0560 0206	JUMP F1	/DO ANOTHER LOOP
787	0561 0550	AGAIN1	
788			
789	0562 0206	A, JUMP F1	/WASTE 2 CYCLES TO SKIP FLUX TRANSITION
790	0563 0535	BACK	
791			
792	0564 0206	B, JUMP F1	/WASTE 2 CYCLES TO SKIP FLUX TRANSITION
793	0565 0554	BACK	
794			
795			
796			
797			
798			
799			

/THIS ROUTINE WRITES THE CONTENTS OF THE SECTOR BUFFER.

800			
801	0566 0022	WRTDAT, SET EGATE	/TURN ON ERASE CURRENT AT START OF DATA FIELD
802	0567 0073	ICT	/NOOP, WASTE 2 CYCLES
803	0570 0073	ICT	/NOOP
804			
805	0571 0170	DATAA, BR WDATA0 ZERO	/WHAT'S THE DATA BIT?
806	0572 0615	C	/ZERO, GO WRITE NOTHING
807			
808	0573 0056	CRC ONE	/ONE, UPDATE THE CRC WITH 1
809			
810	0574 0063	TOG FLAG	/WRITE A DATA TRANSITION
811	0575 0073	ICT	/NOOP FOR BIT CELL TIMING
812			
813	0576 0162	BACK, BR BAROFL T	/DONE ENTIRE SECTOR?
814	0577 0624	WRTCRC	/YES, GO WRITE THE CRC
815			
816	0600 0046	INCR BAR	/NO, BRING UP NEXT DATA BIT FROM SEC BUFFER

817			
818	0601 0070	LCT	/NOOP - WASTE 5 CYCLES WITH
819	0602 0376	-2	/NOOP - A SELF TEST OF THE COUNTER
820	0603 0073	ICT	/NOOP
821	0604 0124	BR COFL F	/NOOP
822	0605 0620	SELF	/NOOP
823			
824	0606 0063	TOG FLAG	/WRITE A CLOCK TRANSITION
825			
826	0607 0270	LCT	/NOOP - WASTE 4 CYCLES WITH
827	0610 0377	-1	/NOOP - A SELF TEST OF THE COUNTER
828	0611 0124	BR COFL F	/NOOP
829	0612 0620	SELF	/NOOP
830			
831	0613 0206	JUMP F1	/GO WRITE ANOTHER DATA BIT
832	0614 0571	DATAA	
833			
834	0615 0054	C, CRC ZERO	/UPDATE CRC WITH 0 AND SKIP DATA TRANSITION
835	0616 0206	JUMP F1	
836	0617 0576	BACK	
837			
838			
839	0620 0070	SELF, LCT	/A SELF DIAGNOSTIC HAS FAILED
840	0621 0060	KSELF	
841	0622 0226	JUMP F5	
842	0623 2610	GOERDN	
843			
844			
845			
846			
847			
848			
849	0624 0070	WRTCRC, LCT	/PRESET BIT COUNTER FOR 16 BITS
850	0625 0357	-16-1	
851			
852	0626 0075	LSR	/NOOP WASTE 4 CYCLES AND SELF TEST THE SR
853	0627 0002	DISK	/NOOP
854	0630 0120	BR SR7 ZERO	/NOOP
855	0631 0620	SELF	/NOOP
856			
857	0632 0063	TOG FLAG	/WRITE A CLOCK TRANSITION
858			
859	0633 0076	ROTATE ONE	/NOOP WASTE 6 CYCLES WITH MORE SELFTEST
860	0634 0076	ROTATE ONE	/NOOP
861	0635 0076	ROTATE ONE	/NOOP
862	0636 0076	ROTATE ONE	/NOOP
863	0637 0120	BR SR7 ZERO	/NOOP
864	0640 0620	SELF	/NOOP
865			
866	0641 0130	BR CRC16 ZERO	/WHAT IS THE CRC BIT
867	0642 0653	D	/ZERO, DO NOT WRITE ANYTHING
868			
869	0643 0056	CRC ONE	/ONE, BRING UP THE NEXT BIT
870			
871	0644 0063	TOG FLAG	/WRITE A DATA TRANSITION

872	0645	0076	ROTATE ONE	/NOOP
873	2646	0273	DRACK, ICT	/BUMP THE BIT COUNTER
875	2647	0126	BR COFL T	/DOIE CRC YET?
876	2650	2656	WRTPTST	/YES, GO WRITE A POSTAMBLE
879	0651	0206	JUMP F1	/NO, GO WRITE ANOTHER CRC BIT
880	0652	2627	E	
881	0653	0054	C, CRC ZERO	/BRING UP NEXT CRC BIT AND SKIP DATA TRANSITION
882	0654	0206	JUMP F1	
883	0655	2646	DRACK	
885				
886				
887				
888				
889				
890				
891				
892				
893	0656	0070	WRTPTST, LCT	/SETUP TO CALL WRT0S TO WRITE 8 BITS OF ZEROES
894	0657	0066	CEGATE	
895	0660	0075	LSR	
896	0661	0070	LCT	
897	0662	0367	-0-1	
898	0663	0063	TOG FLAG	/WRITE LAST CLOCK TRANSITION OF THE CRC FIELD
899				
900	0664	0212	JUMP F2	/CALL THE SUBROUTINE WRITE ZEROES
901	0665	1322	WRT0S	
903				
904	0666	0004	CEGATE, CLR W GATE	/DISABLE WRITE CURRENT
906	0667	0070	LCT	/CALL WRT0S FOR 127 BITS (511.2 MICRO SEC)
907	0670	0076	CEGATE	/DELAY TO ERASE TURN OFF
908	0671	0075	LSR	
909	0672	0070	LCT	
910	0673	0200	-127-1	
911	0674	0212	JUMP F2	
912	0675	1322	WRT0S	
913				
914				
915	0676	0020	CEGATE, CLR EGATE	/DISABLE ERASE CURRENT
916				
917	0677	0070	LCT	/CALL WRT0S FOR 25 BIT (101 MICRO SEC) DELAY
918	0720	0706	READOK	/BEFORE TRYING TO READ
919	0701	0075	LSR	
920	0702	0070	LCT	
921	0703	0346	-25-1	
922	0704	0212	JUMP F2	
923	0705	1322	WRT0S	
924				
925	0706	0070	READOK, LCT	/CALL FIND HEADER ROUTINE TO INSURE
926				

/THIS ROUTINE WRITES THE ONE BYTE POSTAMBLE, TURNS OFF
/WRITE CURRENT, DELAYS 511 MICRO SEC AND TURNS OFF ERASE
/CURRENT. IT UTILIZES THE WRITE ZEROES SUBROUTINE.

927	0707	0712	GODONE	/THAT THE DISK IS STILL MOVING
928	0710	0216	JUMP F3	
929	0711	1400	FINDHD	
930				
931	0712	0212	GODONE, JUMP F2	/WRITE SECTOR FUNCTION IS COMPLETE
932	0713	1006	OKDONE	
933				
934				
935				
936				
937				
938				
939				
940				
941				
942	0714	0270	FINDSE, OPEN RTNA	/SAVE RETURN ADDRESS
943	0715	0075	LSR	
944	0716	0064	LSP	
945				
946	0717	0260	OPEN TEMPG	/PRESET SECTOR TRY COUNT TO 52 TRIES
947	0720	0070	LCT	
948	0721	0313	-52-1	
949				
950	0722	0075	AGAIN2, LSR	/STORE SECTOR TRY COUNT
951	0723	0064	LSP	
952				
953	0724	0070	LCT	/CALL SUBROUTINE TO FIND A HEADER
954	0725	0730	CHKSEC	
955	0726	0216	JUMP F3	
956	0727	1400	FINDHD	
957				
958	0730	0174	CHKSEC, BR FLAGO ZERO	/CORRECT SECTOR? FLAG=1 IF NO
959	0731	0743	WAIT	/YES, GO WAIT FOR PREAMBLE
960				
961	0732	0260	OPEN TEMPG	/NO, RECALL SECTOR TRY COUNT AND INCREMENT IT
962	0733	0071	ESP	
963	0734	0073	ICT	
964				
965	0735	0124	BR COFL F	/52 TRIES MADF FOR SECTOR YET?
966	0736	0722	AGAIN2	/NO, TRY ANOTHER SECTOR
967				
968	0737	0270	LCT	/YES, CANN'T FIND THE SECTOR
969	0740	0070	KNXHDR	
970	0741	0226	JUMP F5	
971	0742	2610	GOERDN	
972				
973	0743	0070	WAIT,	/STALL 323.2 MICRO SECONDS TO WAIT FOR DATA PREAMBLE
974	0744	0345	-26-1	
975	0745	0073	ICT	
976	0746	0124	BR COFL F	
977	0747	0745	-2	
978	0750	0073	ICT	
979	0751	0124	BR COFL F	
980	0752	0750	-2	
981	0753	0073	ICT	

/SUBROUTINE: FINDSECTOR]
/SUBROUTINE TO FIND A SPECIFIC SECTOR. ENTER WITH RETURN ADDRESS
/IN CNTR, DESIRED TRACK ADDRESS IN TARTRK AND DESIRED SECTOR ADDRESS
/IN TARSEC. THIS SUBROUTINE ASSUMES THAT THE TARGET TRACK HAS ALREADY
/BEEN REACHED.


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/RX01 FLOPPY CONTROLLER FIRMWARE      PAL10  VI02A  9-FEB-76  9:17  PAGE 6-7

982  0754 0124  BR COFL F
983  0755 0753  .-2
984
985  0756 0270  OPEN RTNA
986  0757 0203  JUMP F0 IND
987
988
989
990
991  0760 2074  /ROUTINE: READ SECTOR]
992  0761 2074  /ROSEC, ROTATE ZERO
993  0762 0214  ROTATE ZERO
994  0763 0064  OPEN STAT
995
996
997  0764 2070  LCT
998  0765 0770  GOREAD
999  0766 0202  JUMP F0
1000 0767 0103  FINDTR
1001
1002  0770 0222  GOREAD, JUMP F4
1003  0771 2167  READ
1004
1005
1006  0772 0002  /OPEN FREE LOCATIONS
1007  0773 0000  /OPEN
1008  0774 0000  /OPEN
1009  0775 0200  /OPEN
1010  0776 0000  /OPEN
1011  0777 0002  /OPEN

/RETURN FROM THIS SUBROUTINE AT WRITE TURN ON TIME
/OF THE DESIRED SECTOR

/CALL THE FIND TRACK SUBROUTINE TO LOCATE DESIRED SECTOR

/GO READ THE DATA FIELD

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/RX01 FLOPPY CONTROLLER FIRMWARE      PAL10  VI02A  9-FEB-76  9:17  PAGE 9

1012
1013
1014
1015  1002 2220  EPDONE, CLR DONE
1016  1001 0010  CLR XREG
1017
1018  1002 0000  INTERF
1019
1020  1003 0006  SET ERR
1021
1022  1004 0212  JUMP F2
1023  1005 1007  .+2
1024
1025  1006 0204  OKDONE, CLR ERR
1026
1027  1007 0214  OPEN STAT
1028
1029  1010 0071  ESP
1030  1011 0075  LSR
1031
1032  1012 0024  CLR SHIFT
1033  1013 0020  CLR DONE
1034  1014 0010  CLR XREG
1035
1036  1015 0000  INTERF
1037
1038  1016 0030  CLR SECDAT
1039
1040  1017 0016  SET IOOUT
1041
1042  1020 0070  LCT
1043  1021 0367  -B-1
1044  1022 0026  SET SHIFT
1045  1023 0024  CLR SHIFT
1046  1024 0073  ICT
1047  1025 0074  ROTATE ZERO
1048  1026 0124  BR COFL F
1049  1027 1022  .-5
1050
1051  1030 0014  CLR IOOUT
1052
1053  1031 0022  STDONE, SET DONE
1054  1032 0070  LCT
1055  1033 0370  PFUNCT
1056  1034 0222  JUMP F4
1057  1035 2001  GETCMD
1058
1059  1036 0074  FUNCT, ROTATE
1060  1037 0074  ROTATE
1061  1040 0074  ROTATE
1062  1041 0122  BR SP7 ONE
1063  1042 1044  .+2
1064  1043 0061  FLAG OFF
1065
1066  1044 0274  ROTATE

/ROUTINE: DONE AND ERROR DONE]

/SELECT INTERFACE BUSS
/ASSERT ERROR LINE
/SKIP NEXT INSTRUCTION
/NEGATE ERROR LINE
/OPEN STAT TO MOVE TO INTERFACE
/STAT OR ERREG TO SR
/CLEAR INTERFACE OUTPUT BUFFER
/SELECT INTERFACE OUTPUT BUSS
/SELECT SR AS DATA LINE SOURCE
/DEFINE DATA DIRECTION AS OUT (TO INTERFACE)
/MOVE SR TO INTERFACE SERIALY

/NEXT TRANSFER WILL BE FROM INTERFACE
/FUNCTION IS DONE
/CALL GET COMMAND SUBROUTINE TO GET NEXT FUNCTION

/MOVE UNIT SELECT BIT TO SR7
/FLAG IS ALREADY SET. SAVE UNIT IN FLAG, ONE=UNIT 0
/GET FIRST FUNCTION BIT TO SR7

```

1067			
1068	1045 0120	BR SR7 ZERO	
1069	1046 1066	FUNCT4	/FUNCTION 4 OR GREATER
1070			
1071	1047 0074	ROTATE	/GET 2ND FUNCTION BIT
1072			
1073	1050 0120	BR SR7 ZERO	
1074	1051 1057	FUNCT2	/FUNCTION CODE IS 2 OR 3
1075			
1076			
1077	1052 0074	ROTATE	/GET LAST FUNCTION BIT
1078			
1079	1053 0120	BR SR7 ZERO	
1080	1054 1107	EMPTYBUF	/FUNCTION CODE 1
1081			
1082	1055 0212	JUMP F2	/FUNCTION CODE "
1083	1056 1110	FILLBUF	
1084			
1085	1057 0074	FUNCT2, ROTATE	/GET LAST FUNCTION BIT
1086			
1087	1060 0120	BR SR7 ZERO	
1088	1061 1105	PRDSEC	/FUNCT.ON CODE 3
1089			
1090	1062 0070	LCT	/CLR CNTR BITA TO INDICATE NORMAL DATA
1091	1063 0200	0	/FUNCTION 2
1092	1064 0206	JUMP F1	
1093	1065 0400	WRTSEC	
1094			
1095	1066 0074	FUNCT4, ROTATE	/GET 2ND FUNCTION BIT
1096			
1097	1067 0120	BR SR7 ZERO	
1098	1070 1076	FUNCT6	/FUNCTION CODE IS 6 OR GREATER
1099			
1100	1071 0074	ROTATE	/GET LAST FUNCTION BIT
1101			
1102	1072 0120	BR SR7 ZERO	
1103	1073 1224	RDSTAT	/FUNCTION 5
1104			
1105	1074 0212	JUMP F2	/FUNCTION 4-UNUSED
1106	1075 1243	CLRID	
1107			
1108	1076 0074	FUNCT6, ROTATE	/GET LAST FUNCTION BIT
1109			
1110	1077 0120	BR SR7 ZERO	
1111	1100 1275	RDREG	/FUNCTION 7
1112			
1113	1101 0070	LCT	/SET CNTR6 TO INDICATE DELETED DATA
1114		OCTAL	
1115	1122 2127	100	
1116		DECIMAL	
1117	1103 2206	JUMP F1	
1118	1104 0400	WRTSEC	/FUNCTION 6
1119			
1120	1105 0206	PRDSEC, JUMP F1	/POINTER TO READ SECTOR FUNCTION
1121	1106 0760		

1122			
1123			
1124			
1125			
1126			
1127			
1128			
1129			
1130			
1131			
1132	1107 0016	EMPTYBUF, SET IOOUT	/IOOUT IS CLEARED, SET IT TO INDICATE DATA IS MOVING TO THE INTERFACE
1133			
1134			
1135	1110 0074	FILLBUF, ROTATE ZERO	/CLEAR STAT
1136	1111 0274	ROTATE ZERO	
1137	1112 0214	OPEN STAT	
1138	1113 0064	LSP	
1139			
1140	1114 0210	OPEN ERREG	/CLEAR ERREG
1141	1115 0064	LSP	
1142			
1143	1116 0061	FLAG OFF	/NOOP
1144			
1145	1117 0044	CLR BAR SHORT	/ADDRESS THE 1ST BIT OF SECTOR BUFFER
1146			
1147	1120 0070	LCT	
1148	1121 0177	-128-1	/SET UP BYTE COUNT TO 128 (8 BIT) OR 64 (12 BIT)
1149	1122 0150	BR XI18BIT F	
1150	1123 1126	*3	
1151	1124 0070	LCT	
1152	1125 0277	-64-1	
1153	1126 0230	OPEN TEMP4	
1154			
1155	1127 0106	BR I0830T T	/WHICH FUNCTION IS THIS?
1156	1130 1210	EMPTY1	/EMPTYBUF
1157			
1158	1131 0012	XFRD, SET XREQ	/REQUEST DATA TRANSFER
1159			
1160	1132 0073	ICT	/INCREMENT BYTE COUNT AND RESTORE
1161	1133 0075	LSR	
1162	1134 0064	LSP	
1163			
1164	1135 0070	LCT	/CALL WAITRUN S18R TO WAIT FOR DATA TRANSFER
1165	1136 1141	NEWORD	
1166	1137 2222	JUMP F4	
1167	1140 2312	WAITPN	
1168			
1169	1141 0230	NEWORD, OPEN TEMP4	/REOPEN THE BYTE COUNT REGISTER BECAUSE WAITRUN CLOSED IT
1170	1142 0070	LCT	/SET UP BIT COUNT IN CNTR TO 8 BITS OR 12 BITS
1171	1143 0367	-8-1	
1172	1144 0150	BR XI18BIT F	
1173	1145 1150	*3	
1174	1146 0070	LCT	
1175	1147 0363	-12-1	
1176			

```

1177 1150 0104 BR I0B30T F
1178 1151 1175 FILL1
1179
1180
1181 BYTEOUT, SET SHIFT
1182 INCR BAR
1183 CLR SHIFT
1184 ICT
1185 BR COFL F
1186 BYTEOUT
1187
1188 ESP
1189 BR COFL F
1190 XFRQ
1191
1192 SET XREQ
1193
1194 BR RUN F
1195 .-1
1196 CLR XREQ
1197
1198 JUMP F2
1199 OKDONE
1200
1201 FIN WRTBUF
1202
1203 INCR BAR
1204
1205 SET SHIFT
1206 CLR SHIFT
1207
1208 FILL1, START WRTBUF
1209
1210 ICT
1211 BR COFL F
1212 .-7
1213
1214 FIN WRTBUF
1215
1216 INCR BAR
1217
1218 ESP
1219 BR COFL F
1220 XFRQ
1221
1222 JUMP F2
1223 OKDONE
1224
1225 EMPTY1, SET SECDAT
1226
1227 ICT
1228 LSR
1229 LSP
1230
1231

```

/WHICH FUNCTION IS THIS?
 /FILLBUF
 /EMPTYBUF, MOVE A BYTE FROM SECTOR BUFFER
 /TO INTERFACE SERIALY
 /CHECK BYTE COUNT
 /NOT DONE, GO REQUEST A DATA TRANSFER
 /DONE, REQUEST TRANSFER OF LAST BYTE
 /WAIT FOR TRANSFER COMPLETION
 /EMPTYRUF FUNCTION IS COMPLETE
 /END SECTOR BUFR WRT PULSE (800 NS)
 /ADDRESS NEXT CELL OF SECTOR BUFFER
 /SHIFT NEXT BIT FROM INTERFACE
 /START SECTOR BUFR WRT PULSE
 /LAST BIT OF BYTE?
 /NO, DO ANOTHER BIT
 /LAST BIT, END SECTOR BUFR WRT PULSE
 /ADDRESS NEXT CELL OF SECTOR BUFFER
 /CHECK BYTE COUNT
 /NOT DONE, GO GET ANOTHER BYTE
 /DONE FILLBUF FUNCTION
 /SELECT SECTOR BUFR AS DATA LINE SOURCE
 /INCREMENT AND SAVE THE BYTE COUNT

```

1232 1214 0270 LCT
1233 1215 0367 -8-1
1234 1216 2150 BR X118IT F
1235 1217 1152 BYTEOUT
1236 1220 0070 LCT
1237 1221 0363 -12-1
1238
1239 JUMP F2
1240 BYTEOUT
1241
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```

/SET UP THE BIT COUNT TO 8 BITS OR 12 BITS
 /GO MOVE A BYTE TO INTERFACE
 /ROUTINE: READ STATUS
 /SELECT THE SOFT UNIT SCRATCH PAD
 /PRESELECT UNIT ONE
 /WHICH UNIT? FLAG=0=UNIT 1
 /UNIT 1, SKIP UNIT 0 SETUP
 /SELECT UNIT ZERO
 /STORE SOFT UNIT BIT
 /CALL CHECKRDY SUBROUTINE, RETURN TO CLRID
 /CLEAR INIT DONE BIT OF STAT
 /STATUS TO SHIFT REG
 /END AROUND SHIFT OF FIRST 5 BITS

```
1287 1261 1251      *-8
1288 1262 0176      RM FLAG0 T      /IF FLAG IS SET THEN ROTATE IS DONE
1289 1263 1272      GODUN
1291 1264 0062      FLAG ON
1293 1265 0074      RCTATE ZERO
1294 1266 0070      LCT
1295 1267 0375      -2-1
1296 1270 0212      JUMP F2
1297 1271 1251      RCT
1298
1299
1300 1272 2064      LSP      /RESTORE STAT AND GO DONE
1301 1273 0212      JUMP F2
1302 1274 1006      OKDONE
1303
1304      /ROUTINE: READ ERROR REGISTER]
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1275 0210      RDEREG, OPEN ERREG
1276 0212      JUMP F2
1277 1010      OKDONE+2

/([SUBROUTINE: DELAY]. THIS SUBROUTINE PROVIDES DELAYS IN MULTIPLES
/OF .1MS. ENTER WITH RETURN ADDRESS IN THE SHIFT REG.
/AND MULTIPLIER IN THE COUNTER

1300 0264      DELAY, OPEN RTNB      /SAVE THE RETURN ADDRESS
1301 0064      LSP
1302 0075      LSR      /MULTIPLIER TO SHIFT REGISTER
1303 0070      LCT      /DELAY 490 CYCLES (98 MICRO SECONDS)
1304 0205      -122-1
1305 0073      ICT
1306 0264      OPEN RTNB
1307 0124      BR COFL F
1308 1305      *-3
1309      ESP
1310 0071      LSP
1311 0071      ESP
1312 0064      LSP
1313 0075      LSR
1314 0071      ESP
1315 0064      LSP
1316 0073      ICT      /INCREMENT THE MULTIPLIER
1317 0124      BR COFL F      /ANY MORE .1MS LOOPS?
1318 1301      DELAY+1      /YES, GO TO IT
1319 0223      JUMP F4 IND      /NO, RETURN FROM SUBROUTINE
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/([SUBROUTINE: WRITE ZEROS]
/THIS SUBROUTINE WRITES A SPECIFIED NUMBER OF ZEROS IF
/WRITE GATE IS ON. IF WRITE GATE IS OFF IT ACTS AS A
/DELAY OF N.5 BITS. ENTRANCE IS MADE WITH RETURN ADDRESS
/IN THE SR, NUMBER OF BITS IN THE CNTR, AND A CLOCK
/TRANSITION OCCURRING IMMEDIATELY PRIOR TO THE JUMP INTO
/THIS SUBROUTINE.

1322 0274      *RT0S, OPEN RTN      /SAVE RETURN ADDRESS
1323 0064      LSP
1324 0075      LSR      /PUT BIT COUNTER IN SR
1325 0230      OPEN TEMPA      /TEMPO IS THE PATH THROUGH THE SP
1326 0070      LCT      /STALL 2.6 MICRO SECONDS
1327 0374      -3-1
1328 0073      ICT
1329 0124      BR COFL F
1330 1330      *-2
1331 0064      LSP
1332 0071      ESP      /NOOP
1333 0071      ESP      /NOOP
1334 0063      TOG FLAG      /WRITE A CLOCK TRANSITION IF WRT GATE IS SET
1335 0064      LSP
1336 0064      ESP      /PUT BIT COUNT IN THE COUNTER
1337 0071      ICT      /INCREMENT BIT COUNT
1338 0075      LSR      /PUT UPDATED BIT COUNT BACK IN SR
1339 0124      BR COFL F      /DONE ALL BITS?
1340 1326      LOOP      /NO
1341 0274      OPEN RTN      /YES, RETURN FROM SUBROUTINE
1342 0207      JUMP IND F1
1343
1344 0222      PGOTIT, JUMP F4      /POINTER TO GETWORD FROM WAITRUN
1345 2010      GOTIT
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/([ROUTINE: INITIALIZE CONT.]
TEST2, FLAG OFF      /CLEAR FLAG TO INDICATE R10 IS BEING TESTED
TEST1, LCT      /LOOP TO TEST THAT SR IS 252 AND THAT
-5-1      /IT CAN BE SHIFTED.
TSTAGN, BR SR7 ZERO      /TEST FAILURE
INTER1      ROTATE ONE
BR SR7 ONE
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1397	1357	1374	INTER1	/TEST FAILURE
1398	1360	0074	ROTATE ZERO	
1399	1361	0073	ICT	
1400	1362	0124	BR COFL F	
1401	1363	1353	TSTAGN	
1402				
1403	1364	0250	OPEN R10	/CONTENTS OF R10 TO SR. SHOULD BE 125
1404	1365	0071	ESP	
1405	1366	0075	LSR	
1406				
1407	1367	0074	ROTATE ZERO	/SHIFT SR ONCE TO CHANGE 125 TO 252
1408				
1409	1370	0176	BR FLAGO ONE	/HAS R10 BEEN TESTED ALREADY?
1410	1371	1350	TEST2	/NO
1411				
1412	1372	0202	TESTDN, JUMP F0	/YES, RETURN TO REMAINING INITIALIZE ROUTINE
1413	1373	0004	TSTRTN	
1414				
1415	1374	0006	INTER1, SET FHR	/SELF TEST ERROR. SET ERROR AND GO SET DONE
1416	1375	0212	JUMP F2	
1417	1376	1031	STDONE	
1418				
1419	1377	0000	0	/OPE.

1420 /([SUBROUTINE: FINDHEADER AND FIND DATA ADDRESS MARK])
1421 /SUBROUTINE TO LOCATE A LEGAL HEADER (CORRECT CRC AND TRACK #)
1422 /ENTER WITH THE RETURN ADDRESS IN CNTR. ALSO ROUTINE TO FIND A DATA MARK
1423 /OR DELETED DATA MARK.

/THIS ROUTINE LOCATES A SIX BYTE PREAMBLE OF ZEROES.

1427	1400	0264	FINDHD, OPEN RTNB	/STORE RETURN ADDRESS
1428	1401	0075	LSR	
1429	1402	0064	LSP	
1430				
1431	1403	0230	OPEN TEMPA	/256 TO BAD START INNER COUNT
1432	1404	0070	LCT	
1433	1405	0377	-1	
1434	1406	0075	LSR	
1435	1407	0064	LSP	
1436				
1437	1410	0234	OPEN TEMPB	/3 TO CNTR FOR BAD START OUTER COUNT. 768 BAD STARTS ALLOWED
1438	1411	0070	LCT	
1439	1412	0370	-3-1	
1440				
1441	1413	0075	TRYAGN, LSR	/RESTORE BAD START COUNT
1442	1414	0064	LSP	
1443				
1444	1415	0045	CLR BAR LONG	/RESET FOR A COUNT OF 4096 AS PREAMBLE FAILURE COUNT
1445				
1446	1416	0240	OPEN TEMPC	/24 TO CNTR AS ZERO BIT COUNT
1447	1417	0070	LCT	
1448	1420	0347	-24-1	
1449	1421	0075	LSR	/RESTORE ZERO BIT COUNT
1450	1422	0064	LSP	
1451				
1452	1423	0070	LCT	/PUT 0 IN SR7 FOR DATA COMPARISONS, ALSO CONSTANT FOR 40 MICRO SEC WAIT BRANCH
1453	1424	0067	-200-1	
1454	1425	0075	LSR	
1455				
1456	1426	0346	WBR SEPCLK T	/WAIT 40 MICRO SECONDS FOR SEP CLK
1457	1427	1432	+3	
1458				
1459	1430	0216	JUMP F3	/ERROR, NO SEP CLK
1460	1431	1667	TIMERR	
1461				
1462	1432	0154	BR DEOSR7 F	/WHAT IS SEP DATA?
1463	1433	1746	NOZERO	/ONE, GO CHECK PREAMBLE FAILURES
1464				
1465	1434	0071	ESP	/ZERO FOUND, CHECK ZERO COUNT
1466	1435	0073	ICT	
1467	1436	0124	BR COFL F	/NEED MORE ZEROES FOR PREAMBLE
1468	1437	1421	MOREDS	/FOUND PREAMBLE, CLR FLAG TO INDICATE SEARCH FOR IDAM
1469	1440	0061	FLAG OFF	
1470				
1471	1441	0045	GETDAM, CLR BAR LONG	/START SEARCH FOR IDAM OR DATA AM, BAR IS NOSTART COUNTER
1472				
1473	1442	0070	LCT	/WAIT 40 MICRO SEC FOR SEP CLK
1474				

```
1475      1443 0067      -200-1
1476      1444 0346      WBR SEPCLK T
1477      1445 1450      .+3
1478      1446 0216      JUMP F3
1479      1447 1667      TIMERR
1480
1481      1450 0156      BR DECSR7 T
1482      1451 1755      NOTYET
1483
1484      1452 2164      BR MCEQSR F
1485      1453 1673      BADSR7
1486
1487      1454 0057      PRECRC
1488      1455 0056      CRC ONE
1489      1456 2056      CRC ONE
1490
1491      1457 0070      LCT
1492      1460 0067      -200-1
1493      1461 0346      WBR SEPCLK T
1494      1462 1465      .+3
1495      1463 0216      JUMP F3
1496      1464 1667      TIMERR
1497
1498      1465 0156      BR DECSR7 T
1499      1466 1673      BADSR7
1500      1467 0166      BR MCEQSR T
1501      1470 1673      BADSR7
1502
1503      1471 0056      CRC ONE
1504      1472 0056      CRC ONE
1505      1473 0056      CRC ONE
1506
1507      1474 0070      LCT
1508      1475 0067      -200-1
1509      1476 0346      WBR SEPCLK T
1510      1477 1502      .+3
1511      1500 0216      JUMP F3
1512      1501 1667      TIMERR
1513
1514      1502 0154      BR DECSR7 F
1515      1503 1673      BADSR7
1516      1504 0164      BR MCEQSR F
1517      1505 1673      BADSR7
1518
1519      1506 0070      LCT
1520      1507 0000      0
1521      1510 0075      LSR
1522
1523      1511 0070      LCT
1524      1512 0067      -200-1
1525      1513 0346      WBR SEPCLK T
1526      1514 1517      .+3
1527      1515 0216      JUMP F3
1528      1516 1667      TIMERR
1529
```

/DATA SHOULD BE 1, MISSING CLK SHOULD BE T

/JAM 3 MORE CRC BITS

/WAIT FOR THIRD BIT CELL

/DATA SHOULD BE 0, MISSING CLK SHOULD BE F

/CLEAR SR

/WAIT FOR 4TH BIT CELL

```
1530      1517 0154      BR DECSR7 F
1531      1520 1673      BADSR7
1532      1521 0042      LDHD
1533      1522 0042      LDHD
1534      1523 0164      BR MCEQSR F
1535      1524 1673      BADSR7
1536
1537      1525 0070      LCT
1538      1526 0067      -200-1
1539      1527 0346      WBR SEPCLK T
1540      1530 1533      .+3
1541      1531 0216      JUMP F3
1542      1532 1667      TIMERR
1543
1544      1533 0156      BR DECSR7 T
1545      1534 1673      BADSR7
1546
1547      1535 0176      BR FLAGO T
1548      1536 1675      DAM
1549
1550      1537 0164      BR MCEQSR F
1551      1540 1673      BADSR7
1552
1553      1541 0056      CRC ONE
1554
1555      1542 0070      LCT
1556      1543 0067      -200-1
1557      1544 0346      WBR SEPCLK T
1558      1545 1550      .+3
1559      1546 0216      JUMP F3
1560      1547 1667      TIMERR
1561
1562      1550 0156      BR DECSR7 T
1563      1551 1673      BADSR7
1564      1552 0164      BR MCEQSR F
1565      1553 1673      BADSR7
1566
1567      1554 0042      LDHD
1568
1569      1555 0056      CRC ONE
1570
1571      1556 2070      LCT
1572      1557 0067      -200-1
1573      1560 0346      WBR SEPCLK T
1574      1561 1564      .+3
1575      1562 0216      JUMP F3
1576      1563 1667      TIMERR
1577
1578      1564 0156      BR DECSR7 T
1579      1565 1673      BADSR7
1580      1566 0166      BR MCEQSR T
1581      1567 1673      BADSR7
1582
1583      1570 0054      CRC ZERO
1584
```

/DATA SHOULD BE 0, MISSING CLK SHOULD BE F

/NOOP FOR LONG SEP CLOCK

/NOOP FOR LONG SEP CLOCK

/WAIT FOR FIFTH BIT CELL

/DATA SHOULD BE 1

/IF FLAG SET FINISH LOOKING FOR DATA AM

/FINISH IDAM, MISSING CLK SHOULD BE F

/JAM 6TH CRC BIT OF IDAM

/WAIT FOR SIXTH BIT CELL

/DATA SHOULD BE 1, MISSING CLK SHOULD BE F

/NOOP FOR LONG SEP CLOCK

/JAM 7TH CRC BIT OF IDAM

/WAIT FOR SEVENTH BIT CELL

/DATA SHOULD BE 1, MISSING CLK SHOULD BE T

/IDAM FOUND, JAM LAST CRC BIT

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/THIS ROUTINE COMPARES THE HEADER TRACK ADDRESS TO THE
/DESIRED TRACK ADDRESS ON THE FLY. IT IS ENTERED AFTER
/FINDING THE IDAM. ERREG BIT " IS SET IF AN ERROR IS DETECTED.

1571	0220	HDRCON, OPEN TARTRK	/TARGET TRACK ADDRESS TO SR
1572	0071	ESP	
1573	0075	LSR	
1574	0070	LCT	/SET BIT COUNTED TO 0
1575	0367	-8-1	
1576	0144	AGAIN3, BR SEPCLK F	/WAIT FOR BIT CELL
1577	1576	-1	
1600	0156	BR DECSR7 T	/SEP DATA EQUAL TO SR??
1601	1605	+4	/NO, TRACK COMPARE ERROR
1602	0274	ROTATE ZERO	/YES, GET NEXT TRACK ADDRESS BIT
1603	0216	JUMP F3	
1604	1610	+4	/SET ERREG BIT " TO INDICATE TRACK ERROR
1605	0210	OPEN ERREG	
1606	0076	ROTATE ONE	
1607	0004	LSP	/UPDATE THE CRC
1610	0055	DATCRC	
1611	0073	ICT	/INCREMENT AND TEST THE BIT COUNTER
1612	0124	BR COFL F	
1613	1576	AGAIN3	/GO DO NEXT BIT
1614	0070	LCT	/TRACK COMPARED, SET UP BIT COUNTER FOR 0 BYTE
1615	0367	-8-1	
1616	0144	AGAIN4, BR SEPCLK F	/WAIT FOR BIT
1617	1616	-1	
1620	0061	FLAG OFF	/CLEAR FLAG FOR NEXT ROUTINE
1621	0061	FLAG OFF	/NOOP FOR LONG SEP CLK
1622	0061	FLAG OFF	/NOOP FOR LONG SEP CLK
1623	0061	FLAG OFF	/NOOP FOR LONG SEP CLK
1624	0055	DATCRC	/UPDATE CRC
1625	0073	ICT	/INCREMENT AND TEST BIT COUNT
1626	0124	BR COFL F	
1627	1616	AGAIN4	/GO DO ANOTHER BIT

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/THIS ROUTINE COMPARES THE HEADER SECTOR ADDRESS WITH THE
/TARGET SECTOR ADDRESS ON THE FLY. IT IS ENTERED FROM
/THE TRACK COMPARE ROUTINE. A MISMATCH WILL SET THE FLAG.

1630	0224	OPEN TARSEC	/TARGET SECTOR ADDRESS TO SR
1631	0071	ESP	
1632	0075	LSR	
1633	0070	LCT	/SET UP BIT COUNTER FOR 8 BITS
1634	0367	-8-1	
1635	0144	AGAIN5, BR SEPCLK F	/WAIT FOR A BIT
1636	1635	-1	
1637	0156	BR DECSR7 T	/HOW DO THEY COMPARE?
1640	1643	+3	/BAD, GO SET THE FLAG
1641	0216	JUMP F3	/GOOD, SKIP THE ERROR FLAG.
1642	1644	+2	
1643	0062	FLAG ON	/SET FLAG TO INDICATE MISMATCH
1644	0074	ROTATE ZERO	/BRING UP NEXT BIT
1645	0055	DATCRC	/UPDATE THE CRC
1646	0073	ICT	/BUMP THE BIT COUNTER
1647	0124	BR COFL F	/ALL BITS COMPARED?
1650	1635	AGAIN5	/NO, LOOP BACK
1651	0070	LCT	/YES, SETUP TO WAIT FOR END OF
1652	0347	-24-1	/CRC
1653	0144	AGAIN6, BR SEPCLK F	/WAIT FOR BIT
1654	1653	-1	
1655	0074	ROTATE ZERO	/NOOP FOR LONG SEP CLK
1656	0074	ROTATE ZERO	/NOOP FOR LONG SEP CLK
1657	0074	ROTATE ZERO	/NOOP FOR LONG SEP CLK
1660	0074	ROTATE ZERO	/NOOP FOR LONG SEP CLK
1661	0055	DATCRC	/UPDATE CRC
1662	0073	ICT	/BUMP THE BIT COUNTER
1663	0124	BR COFL F	/ALL DONE?
1664	1653	AGAIN6	/NO, LOOP BACK
1665	0226	JUMP F5	/YES, GO CHECK IF CRC IS ALL ZEROS
1666	2515	CKCRC	
1667	0070	TIMERR, LCT	
1670	0110	KTIMERR	/40 MICROSEC PASSED AND NO SEP CLOCK WAS SEEN
1671	0226	JUMP F5	
1672	2612	GOERON	

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1673 0226 BADSR7, JUMP F5
1674 2555 BSR7

DAM,
1675 0166 BR MCEQSR T
1676 1673 BSR7

CRC ZERO
1677 0054 /MISSING CLK SHOULD BE T

LCT
1700 0070 /JAM 6TH CRC BIT OF DATA AM
1701 0067 /WAIT FOR SIXTH BIT CELL
1702 0346 -200-1
1703 1706 WBR SEPCLK T
1704 2216 +3
1705 1667 JUMP F3
TIMERR

BR MCEQSR F
1706 0164 BSR7
1707 1673 LDMO
1710 0042 /NOOP FOR LONG SEP CLK

BR DEQSR7 T
1711 0156 /IF DATA=0 THEN LOOK FOR DELETED DATA AM
1712 1727 DELDAT

CRC ONE
1713 0056 /JAM 7TH BIT OF DATA AM

LCT
1714 0070 /WAIT FOR SEVENTH BIT OF DATA AM
1715 0067 -200-1
1716 0346 WBR SEPCLK T
1717 1722 +3
1718 0216 JUMP F3
1719 1667 TIMERR

CRC ONE
1722 0056 /JAM LAST BIT OF DATA AM

BR DEQSR7 F
1723 0154 /DATA SHOULD BE 1
1724 1742 ENDDAM /FLAG IS SET TO INDICATE NORMAL DATA MARK

JUMP F3
1725 0216 /LAST DATA BIT WAS BAD
1726 1673 BSR7

DEL DAT, CRC ZERO
1727 0054 /JAM 7TH CRC BIT OF DEL DATA AM

LCT
1730 0070 /WAIT FOR 7TH CELL OF DEL DATA AM
1731 0067 -200-1
1732 0346 WBR SEPCLK T
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1750 1733 1736 +3
1751 1734 0216 JUMP F3
1752 1735 1667 TIMERR

FLAG OFF
1753 1736 0061 /CLR FLAG TO INDICATE DELETED DATA MARK

CRC ZERO
1756 1737 0054 /JAM LAST CRC BIT OF DEL DATA AM

BR DEQSR7 F
1758 1740 0154 /DATA SHOULD BE 0
1759 1741 1673 BSR7

ENDDAM, BR MCEQSR F
1761 1742 0164 /MISSING CLK SHOULD BE F FOR BOTH DATA AMS
1762 1743 1673 BSR7

JUMP F4
1764 1744 0222 /GO PICK UP DATA FIELD
1765 1745 2206 DATA

NOZERO, INCR BAR
1746 0046 /INCREMENT AND TEST PREAMBLE FAILURE COUNT
1747 0160 BR BAROFL F
1750 1416 TRYAGN+3

LCT
1751 0070 NXPRAM,
1752 0120 KNXPRAM
1753 0226 JUMP F5
1754 2610 GOERDN

NOTVET, INCR BAR
1755 0046 /INCR AND TEST IDAM OR DATA AM START FAILURE COUNT
1756 0042 LDMO /NOOP FOR LONG SEP CLK
1757 0160 BR BAROFL F
1760 1442 GETDAM+1

LCT
1761 0070 NXIDAM,
1762 0130 KNXIDAM
1763 0226 JUMP F5
1764 2610 GOERDN

PNTRDY, JUMP F2
1765 0212 CLRID
1766 1243 PYSRDY, JUMP F2
1767 0212 CLRID
1770 1243

PNORDY, JUMP F2
1771 0212 OKDONE
1772 1006 JUMP F5
1773 0226 INTRDY
1774 2631

0
1775 0000 /OPEN
1776 0000 /OPEN
1777 0000 /OPEN
1802
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1803 /SUBROUTINES: GETWORD AND GETCOMMAND1
1804 /SUBROUTINE TO GET AN EIGHT BIT WORD FROM THE INTERFACE.
1805 /IF TALKING TO A PDP8 INTERFACE IN 12 BIT MODE, THERE
1806 /WILL BE FOUR MEANINGLESS BITS PRECEDING THE DESIRED EIGHT
1807 /BIT WORD, ENTER THIS SUBROUTINE WITH THE RETURN ADDRESS
1808 /IN THE COUNTER. EXIT WITH THE ONES COMPLEMENT OF THE
1809 /DESIRED WORD IN THE SHIFT REGISTER. PARITY IS COMPUTED AND
1810 /CHECKED ON ALL WORDS.
1811
1812 GETWORD, SET XREQ /REQUEST A WORD FROM INTERFACE
1813
1814 GETCMD, LSR /STASH THE RETURN ADDRESS
1815 OPEN RTNA
1816 LSP
1817
1818 LCT /CALL SUBR WAITON TO WAIT FOR A WORD
1819 PGOTIT
1820 JUMP F4
1821 WAITRN
1822
1823 GOTIT, OFF FLAG /CLEAR FLAG FOR PARITY CHECK
1824
1825 CLR ERR /IN CASE RUN WAS A RESPONSE TO DONE
1826 CLR DONE
1827
1828 LCT /SET UP BIT COUNT IN CNTR. 8 BIT OR 12 BIT
1829 -8-1
1830 BR XIIBIT F
1831 +3
1832 LCT
1833 -12-1
1834
1835 WATDAT, BR DATAIN ONE /WHAT IS THE DATA BIT?
1836 GOTONE /ITS A ONE, GO SAVE IT
1837
1838 BR COFL T /ITS A ZERO, WAS IT THE PARITY BIT (9TH BIT)?
1839 CHKPAR /YES, GO CHECK PARITY
1840
1841 ROTATE ONE /NO SAVE THE DATA BIT COMPLIMENTED IN SR
1842
1843 JUMP F4 /GO SHIFT UP ANOTHER BIT.
1844 NUTHER
1845
1846
1847
1848
1849
1850 GOTONE, TOG FLAG /COMPLIMENT THE PARITY GENERATOR
1851
1852 BR COFL T /WAS IT THE PARITY BIT?
1853 CHKPAR /YES, GO CHECK PARITY
1854
1855 ROTATE ZERO /NO, SAVE THE COMPLIMENTED DATA BIT IN SR
1856
1857 NUTHER, SET SHIFT /SHIFT PULSE AND INCREMENT BIT COUNT

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1858 ICT CLR SHIFT
1859
1860 JUMP F4 /GO TEST THIS BIT.
1861 WATDAT
1862
1863
1864
1865
1866 CHKPAR, BR FLAGO ONE /WHERE THERE AN ODD NO. OF ONES?
1867 GOTWRD /YES, PARITY WAS GOOD
1868
1869 OPEN STAT /NO, STAT TO SR
1870 ESP
1871 LSR
1872
1873 LCT /END AROUND SHIFT OF UPPER 5 BITS OF STAT IN SR
1874 -5-1
1875 BR SR7 T
1876 +4
1877 ROTATE ZERO
1878 JUMP F4
1879 +2
1880 ROTATE ONE
1881 ICT ROTATE ONE
1882 BR COFL F
1883 -8
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1885 ROTATE ZERO /CLEAR INIT DONE
1886 ROTATE ONE /SET PARITY ERROR
1887
1888 BR SR7 T /END AROUND SHIFT OF CRC ERROR BIT OF STAT IN SR
1889 +4
1890 ROTATE ZERO
1891 JUMP F4
1892 +2
1893 ROTATE ONE
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1895 LSP /RESTORE STAT TO SCRATCH PAD
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1897 LCT /ERRORCODE FOR PARITY ERROR
1898 KPARER
1899 JUMP F5
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1903
1904 /([SUBROUTINE: STEPHEAD])
1905 /THIS SUBROUTINE WILL STEP THE SPECIFIED NUMBER OF TRACKS IN THE
1906 /SPECIFIED DIRECTION. DIRECTION IS DETERMINED BY THE HD DIR FLOP
1907
1908 /THE NUMBER OF STEPS IS IN THE SR. RETURN ADDRESS IS IN THE CNTR.
1909 /EXIT IS TO THE RETURN ADDRESS IF HOME IS DETECTED. EXIT IS TO RETURN
1910 /PLUS 2 IF THE LAST STEP HAS BEEN TAKEN. AFTER THE LAST STEP IS TAKEN,
1911 /THE HEAD IS LOADED AND A 25MS DELAY IS EXECUTED FOR HEAD SETTLE TIME
1912
1913
1914
1915

2100	0270	STEPHD, OPEN RTNA	/STORE RETURN ADDR AND MOVE STEP COUNT TO CNTR
2101	0064	LSP	
2102	0075	LSR	
2103	0071	ESP	
2104	0064	LSP	
2105	0136	CKHOME, BR HOME T	/IS THE HEAD HOME?
2106	2150	OUT	/YES, GO EXIT
2107	0073	ICT	/NO, INCREMENT STEP COUNT AND STORE IN TEMPA
2110	0075	LSR	
2111	0230	OPEN TEMPA	
2112	0064	LSP	
2113	0070	LCT	/PASS 30 TO DELAY SUBR FOR 3MS DELAY
2114	2124	SECPLS	
2115	0075	LSR	
2116	0070	LCT	
2117	0341	-30-1	
2120	0012	SET STPHD	/ISSUE STEP PULSE
2121	0010	CLR STPHD	
2122	0212	JUMP F2	/CALL DELAY SUBR
2123	1300	DELAY	
2124	0012	SECPLS, SET STPHD	/ISSUE SECOND STEP PULSE
2125	0010	CLR STPHD	
2126	0070	LCT	/CALL DELAY FOR 3MS DELAY
2127	2135	DONSTP	
2130	0075	LSR	
2131	0070	LCT	
2132	0341	-30-1	
2133	0212	JUMP F2	
2134	1300	DELAY	
2135	0230	DONSTP, OPEN TEMPA	/CHECK STEP COUNT
2136	0071	ESP	
2137	0124	BR COFL F	
2140	2105	CKHOME	/NOT DONE, GO CHECK IF HOME

1958	2141	0270	OPEN RTNA	/DONE STEPPING, INCREMENT RETURN ADDRESS BY 2
1959	2142	0071	ESP	
1960	2143	0073	ICT	
1961	2144	0073	ICT	
1962	2145	0270	OPEN RTNA	/STORE RETURN ADDRESS ALSO START OF 25MS DELAY SUBROUTINE
1963	2146	0075	LSR	
1964	2147	0064	LSP	
1966	2150	0042	LDHD	/LOAD HEAD
1967	2151	0250	OPEN TEMPE	/SET SOFT HD LOAD BIT
1968	2152	0070	LCT	
1969	2153	0200	OCTAL	
1970	2154	0075	DECIMAL	
1971	2155	0064	LSR	
1972	2156	0070	LCT	/CALL DELAY SUBR FOR 25MS DELAY
1973	2157	2165	DONDLY	
1974	2160	0075	LSR	
1975	2161	0070	LCT	
1976	2162	0000	-255-1	
1977	2163	0212	JUMP F2	
1978	2164	1300	DELAY	
1979	2165	0270	DONDLY, OPEN RTNA	/RETURN FROM STEP HEAD OR DELAY 25MS SUBROUTINE
1980	2166	0203	JUMP F0 IND	
1981	2167	0070	READ, LCT	/([ROUTINE: READ SECTOR CONT.])
1982	2170	0374	-3-1	/3 TO DATA MARK TRY COUNTER
1983	2171	0234	OPEN TEMPB	
1984	2172	0075	LSR	
1985	2173	0064	LSP	
1986	2174	0070	LCT	/STALL FOR 96 MICRO SEC (3 BYTES) TO AVOID WRT TURN ON SPLASH
1987	2175	0207	-120-1	
1988	2176	0073	ICT	/SET THE FLAG TO SPECIFY DATA AM IN FIND AM ROUTINE
1989	2177	0062	FLAG ON	
1990	2200	0124	BR COFL F	
1991	2201	2176	-3	
1992	2202	0073	ICT	/CLR COUNTER AND SR
1993	2203	0075	LSR	
1994	2204	0216	JUMP F3	/GO TRY FIND THE ADDRESS MARK
1995	2205	1441	GETDAM	

```
2013 /THIS ROUTINE FOLLOWS THE DISCOVERY OF A DATA MARK OR
2014 /A DELETED DATA MARK. IT MOVES THE NEXT 1024 BITS
2015 /INTO THE SECTOR BUFFER, THEN PICKS UP AND CHECKS THE CRC.
2016
2017
2018
2019 DATA, CLR BAR /CLEAR THE BUFFER ADDRESS REGISTER
2020 BR SEPCLK F /WAIT FOR CLOCK
2021 .-1
2022
2023 START *RTBUF /START THE WRITE PULSE FOR THIS BIT
2024
2025 DATCRC /UPDATE THE CRC WITH SEP DATA
2026
2027 BR BAROFL T /IS BUFFER FULL YET?
2028 GETCRC /YES, GO GET THE CRC
2029
2030 FIN *RTBUF /NO, END THE WRITE PULSE
2031
2032 INCR BAR /ADDRESS NEXT SECTOR BUFFER CELL
2033
2034 JUMP F4 /LOOP BACK FOR NEXT BIT
2035 DATA+1
2036
2037 GETCRC, FIN *RTBUF /END THE WRITE PULSE FOR THE LAST BIT
2038
2039 LCT /SET BIT COUNT TO 16 FOR 2 BYTE CRC
2040 -16-1
2041
2042 BR SEPCLK F /WAIT FOR NEXT BIT
2043 .-1
2044
2045 LDHD /4 NOOPS FOR LONG SEP CLOCK
2046 LDHD
2047 LDHD
2048 LDHD
2049 LDHD
2050
2051 DATCRC /PUT CRC BIT IN THE CRC GENERATOR
2052 ICT /INCREMENT AND TEST BIT COUNT
2053 BR COFL F /NOT DONE, GET ANOTHER
2054 .-9
2055 OPEN STAT /STATUS TO SHIFT REG
2056 ESP
2057 LSR
2058
2059 BR SR7 T /END AROUND SHIFT OF DRV RDY BIT OF STAT IN SR
2060 .+4
2061 ROTATE ZERO
2062 JUMP F4
2063
2064 .+2
2065 ROTATE ONE
2066
2067 BR FLAGO T /SET DEL DATA BIT OF STAT IF FLAG=0
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/RX01 FLOPPY CONTROLLER FIRMWARE PAL10 V142A 9-FEB-76 9117 PAGE 12-3
2068 .+4
2069 ROTATE ONE
2070 JUMP F4
2071 .+2
2072 ROTATE ZERO
2073
2074 LCT
2075 -5-1
2076 BR SR7 T
2077 .+4
2078 ROTATE ZERO
2079 JUMP F4
2080 .+2
2081 ROTATE ONE
2082 ICT
2083 BR COFL F
2084 .-8
2085
2086 LCT /SET BIT COUNT TO 16 FOR CRC TEST
2087 -16-1
2088
2089 BR CRC16 ONE /IS THIS CRC BIT OK
2090 DCR CER /NO, GO REPORT DATA CRC ERROR
2091
2092 CRC ZERO /YES, BRING UP NEXT CRC BIT
2093
2094 ICT /INCREMENT AND TEST BIT COUNT
2095 BR COFL F
2096 .-5
2097
2098 ROTATE ZERO /CRC WAS GOOD, CLR CRC ERR BIT OF STAT IN SR
2099 LSP /PUT THE STATUS WORD BACK IN SCRATCHPAD
2100
2101 JUMP F2 /EXIT TO DONE
2102 OKDONE
2103
2104 DCR CER, ROTATE ONE /INSERT 1 INTO CRC ERROR BIT
2105
2106 LSP /PUT THE STAT WORD BACK
2107
2108 LCT /ERROR CODE FOR CRC ERROR
2109 KDCR CER
2110 JUMP F5
2111 GJERN
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/(SUBROUTINE: WAIT FOR RUN)
/THIS SUBROUTINE WILL WAIT FOR RUN. IF 46MS ELAPSES, THE HEAD IS UNLOADED
/AND THE ROUTINE CONTINUES WAITING FOR RUN. RETURN ADDRESS IS PASSED
/VIA THE COUNTER

2312	0264	WAITRN, OPEN RTNB	/STASH THE RETURN ADDRESS
2313	0075	LSR	
2314	0064	LSP	
2315	0102	BR RUN T	/GOT RUN?
2316	2347	GOTRUN	
2317	0240	OPEN TEMPC	/PRESET LOOP COUNTER TO 0
2320	0070	LCT	
2321	0000	0	
2322	0075	BACK, LSR	/RESTORE LOOP COUNT
2323	0064	LSP	
2324	0302	WBR RUN T	/TIME WHILE WAITING FOR FUN
2325	2347	GOTRUN	
2326	0302	WBR RUN T	
2327	2347	GOTRUN	
2328	0302	WBR RUN T	
2329	2347	GOTRUN	
2330	0302	WBR RUN T	
2331	2347	GOTRUN	
2332	0302	WBR RUN T	
2333	2347	GOTRUN	
2334	0071	ESP	/INCREMENT AND TEST LOOP COUNT
2335	0073	ICT	
2336	0124	BR COFL F	
2337	2322	BACK	/46MS NOT ELAPSED YET
2340	0250	OPEN TEMPE	/TIME IS EXPIRED (45.0 MS). CLEAR THE SOFT HOLD BIT AND UNLOAD THE HEAD
2341	0073	ICT	
2342	0075	LSR	
2343	0064	LSP	
2344	0040	UNHD	
2345	0100	BR RUN F	/WAIT FOR RUN. FOREVER IF NECESSARY
2346	2345	0-1	
2347	0010	GOTRUN, CLR XREQ	/IF RUN WAS RESPONSE TO XFREQ
2350	0264	OPEN RTNB	/RETURN FROM WAITRN SUBROUTINE
2351	0213	JUMP IND F2	

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/(ROUTINE: INITIALIZE CONT.)
/CONTINUATION OF THE INITIALIZE SELF TEST

2352	0070	TEST, LCT	/LOAD R5 WITH TEST PATTERN 252
2353	0252	OCTAL	
2354	0075	DECIMAL	
2355	0224	LSR	
2356	0064	OPEN R5	
2357	0070	LSP	
2360	0125	LCT	/LOAD R10 WITH TEST PATTERN 125
2361	0075	OCTAL	
2362	0250	125	
2363	0064	DECIMAL	
2364	0062	LSR	
2365	0176	OPEN R10	
2366	2371	LSP	
2367	0212	FLAG ON	/SET FLAG AND TEST IT
2370	1374	BR FLAGO T	
2371	0224	0-3	
2372	0071	JUMP F2	/FLAG FAILURE
2373	0075	INTER1	
2374	0224	OPEN R5	/CONTENTS OF R5 TO SR. SHOULD BE 252
2375	0071	ESP	
2376	0075	LSR	
2377	0212	JUMP F2	/GO CONTINUE INIT TEST IN FLD 2
2378	1351	TEST1	
2379	0000	0	
2380	0000	0	/OPEN
2381	0000	0	/OPEN

2197 /SUBROUTINE: MAGNITUDE COMPARISON]
2198 /THIS SUBROUTINE COMPARES THE EIGHT BIT NUMBERS IN REGISTERS F AND G
2199 /EXIT IS TO THE RETURN ADDRESS IF F<G. IF F<G, RETURN IS TO RTNA+2.
2200 /IF F>G, RETURN IS TO RTNA+4. CONTENTS OF F AND G ARE UNDEFINED AT
2201 /THE END OF THE SUBROUTINE

2202	2400	0230	MAGCOM, OPEN TEMP	/FOR BIT COUNT
2203	2401	0070	LCT	/BIT COUNT IS 8
2204	2402	0367	-8-1	
2205	2403	0075	LSR	/RESTORE BIT COUNT
2206	2404	0064	LSR	
2207	2405	0254	OPEN TEMPF	/F TO SR
2208	2406	0071	ESP	
2209	2407	0075	LSR	
2210	2410	0120	BR SR7 ZERO	/TEST F
2211	2411	2443	TSTG0	/ITS 0
2212	2412	0076	ROTATE ONE	/ITS 1, BRING UP NEXT BIT
2213	2413	0064	LSR	/RESTORE F
2214	2414	0260	OPEN TEMPG	/G TO SR
2215	2415	0071	ESP	
2216	2416	0075	LSR	
2217	2417	0120	BR SR7 ZERO	/TEST G
2218	2420	2432	GLESSF	/ITS 0, G IS LESS THAN F
2219	2421	0074	NEXTG, ROTATE ZERO	/ITS 1, BRING UP NEXT G BIT
2220	2422	0064	LSR	/RESTORE G
2221	2423	0230	OPEN TEMP	/INCREMENT AND TEST BIT COUNT
2222	2424	0071	ESP	
2223	2425	0073	ICT	
2224	2426	0124	BR COFL F	/GO COMPARE ANOTHER BIT
2225	2427	2403	MAGCOM+3	
2226	2430	0270	OPEN RTNA	/ALL BITS COMPARED, NO DIFFERENCE
2227	2431	0203	JUMP F0 IND	
2228	2432	0270	GLESSF, OPEN RTNA	/G IS LESS THAN F RETURN TO RTNA +4
2229	2433	0071	ESP	
2230	2434	0073	ICT	
2231	2435	0073	ICT	
2232	2436	0073	ICT	
2233	2437	0073	ICT	
2234	2440	0075	LSR	

2252	2441	0064	LSP	
2253	2442	0203	JUMP F0 IND	
2254	2443	0074	TSTG0, ROTATE ZERO	/F WAS 0, BRING UP NEXT BIT
2255	2444	0064	LSR	/RESTORE F
2256	2445	0260	OPEN TEMPG	/G TO SR
2257	2446	0071	ESP	
2258	2447	0075	LSR	
2259	2450	0120	BR SR7 ZERO	/TEST G
2260	2451	2421	NEXTG	/MATCHS F, GO BRING UP NEXT G BIT
2261	2452	0270	OPEN RTNA	/G IS LESS THAN F. RETURN TO RTNA +2
2262	2453	0071	ESP	
2263	2454	0226	JUMP F5	
2264	2455	2436	GLESSF+4	

/SUBROUTINE: FIND TRACK CONT.]

2274	2456	0070	HOMERR, LCT	/HOME FOUND BEFORE LAST STEP TAKEN
2275	2457	0050	KHOMERR	
2276	2460	0226	JUMP F5	
2277	2461	2610	GOERON	

2279 /SUBROUTINE: DIFFERENCE]
2280 /THIS SUBROUTINE COMPUTES THE DIFFERENCE BETWEEN TWO EIGHT BIT
2281 /NUMBERS. ENTER WITH THE RETURN ADDRESS IN RTN, A IN THE
2282 /COUNTER, AND B IN THE SHIFT REGISTER. EXIT IS MADE WITH THE
2283 /COMPLIMENT OF THE DIFFERENCE IN THE SHIFT REGISTER.
2284 /EXIT IS TO RTN IF A>=B. EXIT IS TO RTN+2 IF A<B

2291	2462	0230	DIF, OPEN TEMP	/OPEN TEMPORARY PATH THRU THE SP
2292	2463	0120	BR COFL T	/HAS A REACHED ALL ONES YET?
2293	2464	2501	DIF0	/YES, GO GET A FOR THE DIFFERENCE
2294	2465	0064	LSR	/NO, GET B
2295	2466	0075	LSR	/A INTO SHIFT REG
2296	2467	0071	ESP	/B INTO COUNTER
2297	2470	0126	BR COFL T	/HAS B REACHED ALL ONES YET?
2298	2471	2503	DIFA	/YES, GO GET A FOR THE DIFFERENCE
2299	2472	0073	ICT	/INCREMENT B
2300	2473	0064	LSR	/, BRING BACK A
2301	2474	0275	LSR	/B INTO SHIFT REG
2302	2475	0071	ESP	/A INTO COUNTER

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2307 2476 0073      ICT
2308 2477 0226      JUMP F5
2309 2500 2403      DIF+1
2310
2311
2312 2501 0270      DIFB, OPEN RTNA
2313 2502 0203      JUMP F0 IND
2314
2315
2316 2503 0270      DIFA, OPEN RTNA
2317 2504 0071      ESP
2318 2505 0073      ICT
2319 2506 0073      ICT
2320
2321 2507 0064      LSP
2322 2510 0075      LSR
2323 2511 0071      ESP
2324 2512 0064      LSP
2325 2513 0075      LSR
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2327 2514 0203      JUMP F0 IND
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/ROUTINE: FIND HEADER CONT.]
 /THIS ROUTINE CHECKS THE CRC, AND THE RESULTS OF THE TRACK
 /AND SECTOR COMPARISONS.

```

2515 0070      CKMCRC, LCT
2516 0357      -16-1
2517 0132      BR CRC16 ONE
2520 2546      HRCRCR
2521 0073      ICT
2522 0054      CRC ZERO
2523 0124      BR COFL F
2524 2517      .-5
2525 0210      OPEN ERREG
2526 0071      ESP
2527 0075      LSR
2530 0070      LCT
2531 0370      -7-1
2532 0074      ROTATE ZERO
2533 0073      ICT
2534 0124      BR COFL F
2535 2532      .-3

```

/PRESET BIT COUNT TO 16 FOR CRC
 /IS CRC ZERO
 /NO, LOG ERROR AND TRY AGAIN
 /YES, CRC GOOD SO FAR, BUMP BIT CNTR
 /BRING UP NEXT CRC BIT
 /ALL BITS TESTED?
 /NO, BRANCH BACK
 /YES, CRC WAS GOOD, CHECK TRK COMP
 /ROTATE BIT 0 TO BIT 7
 /DONE ROTATING?
 /NO

```

2362 2536 0122      BR SR7 ONE
2363 2537 2542      TSKSKR
2364
2365 2540 0264      OPEN RTNR
2366 2541 0207      JUMP F1 IND
2367
2368
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2371 2542 0070      TSKSKR, LCT
2372 2543 0150      KTKSKR
2373 2544 0226      JUMP F5
2374 2545 2610      GOERDN
2375
2376
2377 2546 0070      HRCRCR, LCT
2378 2547 0140      KHRCRCR
2379 2550 0075      LSR
2380 2551 0210      OPEN ERREG
2381 2552 0064      LSP
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2383 2553 0226      JUMP F5
2384 2554 2557      RADHDR
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/YES, WAS THERE A BAD COMPARE
 /YES, GO REPORT A TRACK SEEK ERROR
 /CORRECT TRACK, EXIT FROM FIND HDR SUBR

/HEADER CRC WAS GOOD BUT TRACK
 /ADDRESS DID NOT COMPARE. MUST
 /EXIT TO ERROR NONE

/HEADER CRC WAS NOT CORRECT

/LOG THE ERROR

/GO TRY ANOTHER HEADER

/BAD START ON DATA AM OR IDAM?

/IDAM, INCREMENT AND TEST BAD START INNER COUNT

/NO OVERFLOW, GO TRY ANOTHER HEADER
 /INCREMENT AND TEST BAD START OUTER COUNT

/NO OVERFLOW, GO TRY AGAIN
 /TOO MANY TRIES FOR A HEADER

/BAD START ON DATA AM, INCREMENT AND TEST BAD START COUNT

/NO OVERFLOW GO TRY FOR DATA AM AGAIN


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/RX01 FLOPPY CONTROLLER FIRMWARE      PAL10  V142A  9-FEB-76      9:17      PAGE 15-4
2417      2606 0070      NODAM,      LCT
2418      2607 0170      KNODAM
2419      2610 0210      GOERDN, OPEN ERREG
2420      2611 0075      LSR
2421      2612 0064      LSP
2422      2613 0212      JUMP F2
2423      2614 1000      ERDNE
2424
2425      2615 0216      PTRVAG, JUMP F3
2426      2616 1413      TRYAGN
2427
2428
2429      2617 0216      PGETDA, JUMP F3
2430      2620 1441      GETDAM
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2435      2621 0070      /ROUTINE: INITIALIZE CONT.]
2436      2622 0030      WRONG,      LCT
2437      2623 0226      K*RONG
2438      2624 2610      JUMP F5
2439      2625 0070      GOERDN
2440      2626 1771      DNRCAL,      LCT
2441      2627 0226      PNORDY
2442      2630 2640      JUMP F5
2443      2631 0070      CHKRDY
2444
2445      2631 0070      INTRDY,      LCT
2446      2632 0770      GCREAD
2447      2633 0274      OPEN RTN
2448      2634 0075      LSR
2449      2635 0064      LSP
2450      2636 0202      JUMP F0
2451      2637 0252      BOOT
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/RX01 FLOPPY CONTROLLER FIRMWARE      PAL10  V142A  9-FEB-76      9:17      PAGE 16
2456      /SUBROUTINE: CHECKREADY]
2457
2458      /SUBROUTINE TO CHECK THE SELECTED DRIVE TO SEE IF THE
2459      /DISK IS INSERTED AND UP TO SPEED. THIS IS DONE BY CHECKING TO SEE IF
2460      /THE INTERVAL BETWEEN 2 INDEX PULSES IS BETWEEN 150 MS AND 100 MS. RETURN
2461      /ADDRESS IS PLACED IN THE COUNTER BEFORE ENTRY. NOT READY RETURN IS
2462      /TO THE RETURN ADDRESS. READY RETURN IS TO THE RETURN ADDRESS PLUS 2
2463
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2466      /
2467      2640 0274      /CHKRDY, OPEN RTN
2468      2641 0075      /SAVE RETURN ADDRESS
2469      2642 0064      LSR
2470      2643 0070      LCT
2471      2644 0375      -2-1
2472
2473      2645 0230      OPEN TEMPA
2474
2475      2646 0075      NEMPAS,      LSR
2476      2647 0064      LSP
2477
2478      2650 0061      FLAG OFF
2479
2480      2651 0042      LDHD
2481
2482      2652 0070      LCT
2483      2653 0360      -15-1
2484
2485      2654 0234      STDLY,      OPEN TEMPB
2486      2655 0075      LSR
2487      2656 0064      LSP
2488
2489      2657 0070      LCT
2490      2660 0327      -40-1
2491
2492      2661 0240      OPEN TEMPC
2493      2662 0075      SPBACK,      LSR
2494      2663 0064      LSP
2495
2496      2664 0070      LCT
2497      2665 0005      -250-1
2498      2666 0116      BR INDX T
2499      2667 2714      SAWIND
2500      2670 0073      ICT
2501      2671 0124      AR COFL F
2502      2672 2666      *-4
2503
2504      2673 0240      OPEN TEMPC
2505      2674 0071      ESP
2506      2675 0073      ICT
2507      2676 0124      AR COFL F
2508      2677 2662      SPBACK
2509
2510

```

```

/RX01 FLOPPY CONTROLLER FIRMWARE          PAL10  V142A  9-FEB-76      9:17      PAGE 16-1
2511 2700 0234 OPEN TEMPB
2512 2701 0071 ESP
2513 2702 0073 ICT
2514 2703 0124 BR COFL F
2515 2704 2655 STDLY+1
2516
2517 2705 0176 BR FLAGO ONE
2518 2706 2767 UNRDY
2519
2520 2707 0062 FLAG ON
2521
2522 2710 0070 LCT
2523 2711 0374 -3-1
2524
2525 2712 0226 JUMP F5
2526 2713 2654 STDLY
2527
2528
2529
2530 SAWIND, OPEN TEMPB
2531 2715 0071 ESP
2532 2716 0073 ICT
2533 2717 0124 BR COFL F
2534 2720 2646 NEWPAS
2535
2536 2721 0174 BR FLAGO ZERO
2537 2722 2767 UNRDY
2538
2539 2723 0274 OPEN RTN
2540 2724 0071 ESP
2541 2725 0073 ICT
2542 2726 0073 ICT
2543 2727 0075 LSR
2544 2730 0064 LSP
2545
2546 2731 0214 OPEN STAT
2547 2732 0071 ESP
2548 2733 0075 LSR
2549
2550 2734 0076 ROTATE ONE
2551
2552 2735 0061 FLAG OFF
2553
2554 ROT3, LCT
2555 -3-1
2556 BR SR7 T
2557 +4
2558 ROTATE ZERO
2559 JUMP F5
2560 +2
2561 ROTATE ONE
2562 ICT
2563 BR COFL F
2564 -8
2565 BR FLAGO T
/WAS IT FIRST 3 OR LAST 3

```

```

/RX01 FLOPPY CONTROLLER FIRMWARE          PAL10  V142A  9-FEB-76      9:17      PAGE 16-2
2566 2752 2764 EXCHRY
2567
2568 2753 0140 BR WR TEN F
2569 2754 2760 +4
2570 ROTATE ZERO
2571 2755 0074 JUMP F5
2572 2756 0226 +2
2573 2757 2761 ROTATE ONE
2574 2760 0076
2575 2761 0062 FLAG ON
2576 2762 0226 JUMP F5
2577 2763 2736 ROT3
2578
2579 EXCHRY, LSP
2580 2764 0064
2581 2765 0274 OPEN RTN
2582 2766 0217 JUMP F3 IND
2583
2584 UNRDY, OPEN STAT
2585 2767 0214 ESP
2586 2770 0071 LSR
2587 2771 0075 ROTATE ZERO
2588 2772 0074
2589
2590 2773 0226 JUMP F5
2591 2774 2735 ROT3-1
2592
2593 2775 0000 0
2594 2776 0000 0
2595 2777 0000 0
2596
2597
S

```


/RX01 FLOPPY CONTROLLER FIRMWARE

PAL10

V142A

9-FEB-76

9:17

PAGE 16-5

WHCHDR 0075
WRONG 2621
WRT09 1322
WRTCRC 0624
WRT0AM 0514
WRTDAT 0566
WRTPST 0656
WRTSEC 0600
XFRQ 1131
XSTRYS 2573

ERTK 0202
EXCHRY 2764
FILL1 1175
FILLBU 1110
FINDHD 1400
FINDSE 0714
FINDTR 0103
FUNCT 1036
FUNCT2 1057
FUNCT4 1066
FUNCT6 1076
GETCHD 2001
GETCRC 2221
GETDAM 1441
GETWRD 2000
GLESSF 2432
GODONE 0712
GODUN 1272
GOERON 2610
GOREAD 0770
GOTIT 2010
GOTONE 2032
GOTRUN 2347
GOTWRD 2076
MCRCER 2546
HRCOM 1571
H0SETL 0322
HLFDLY 0466
HOMERR 2456
ILTRK 0206
IN10 0045
INTER1 1374
INTRDY 2631
LOOP 1326
MAGCOM 2400
MOREOS 1421
NEWORD 1141
NEWPAS 2646
NEXTG 2421
NODAM 2606
NOSTPS 0357
NOTYET 1755
NOZERO 1746
NUTHER 2034
NXDRV0 0064
NXDRV1 0070
NXHOR 0737
NXIDAM 1761
NXPRAM 1751
OKDONE 1006
OUT 2150
PDHRCCL 0372

0562
ABACK 0535
ABV43 0344
AGAIN 0531
AGAIN1 0550
AGAIN2 0722
AGAIN3 1576
AGAIN4 1616
AGAIN5 1635
AGAIN6 1653
B 0564
BACK 2322
BADDAP 2577
BADHDR 2557
BADSRT 1673
BACK 0554
BSRT 2555
BOOT 0252
BYTEOU 1152
C 0615
CBACK 0576
CEGATE 0676
CFINSE 0351
CHKPAR 2041
CHKRDY 2640
CHKSEC 0730
CHKCRC 2515
CKHOME 2105
CLR10 1243
CKGATE 0666
D 0653
DAM 1675
DAMSUP 0460
DATA 2206
DATAA 0571
DBACK 0646
DCRCER 2304
DELAY 1300
DELDAT 1727
DIF 2462
DIFA 2503
DIFB 2501
DLY25 2145
DNRCAL 2625
DONDLY 2165
DONSTP 2135
DUNSTP 0305
E 0627
EMPTY1 1210
EMPTYB 1107
ENDDAM 1742
ERDNE 1000

/RX01 FLOPPY CONTROLLER FIRMWARE

PAL10

V142A

9-FEB-76

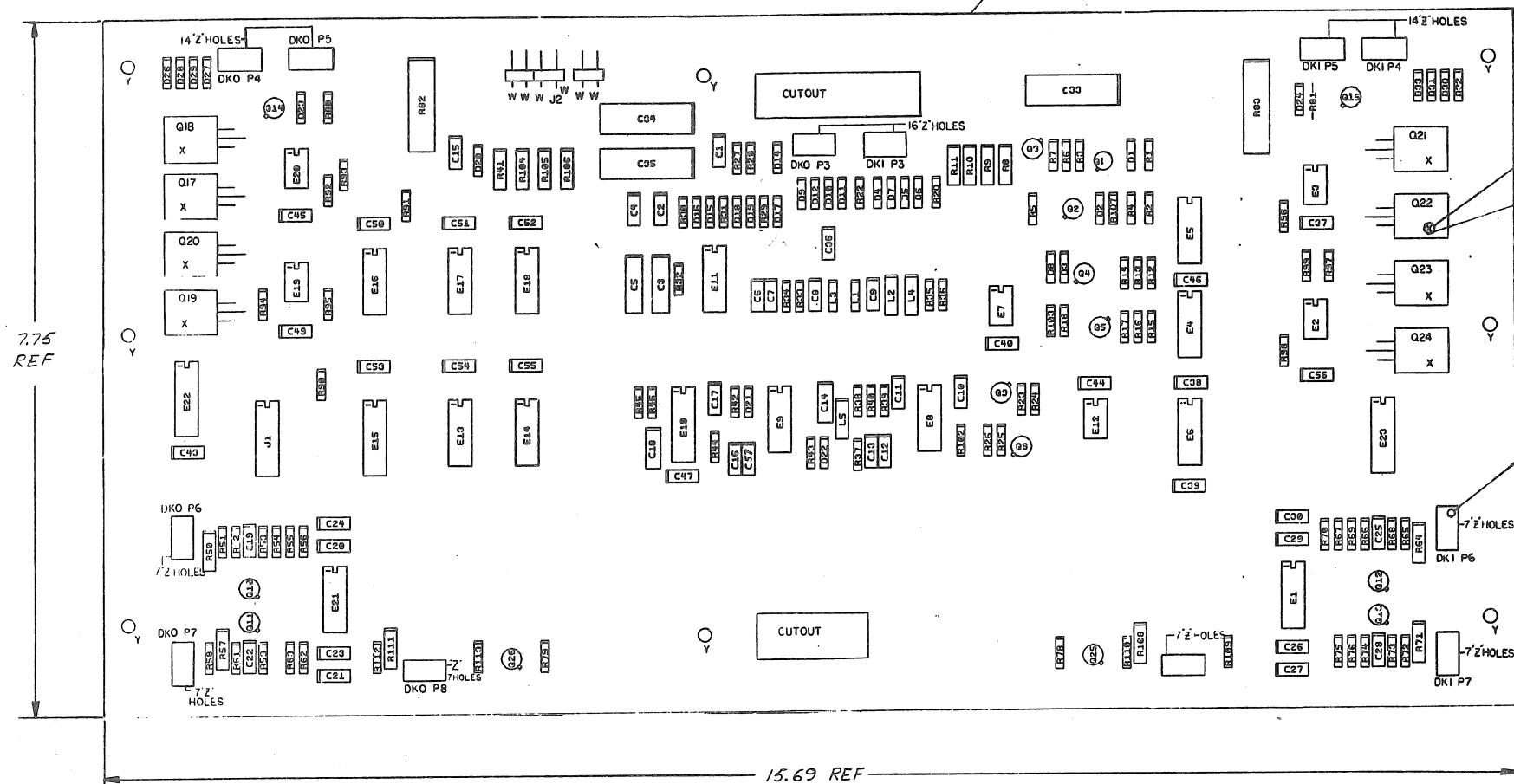
9:17

PAGE 16-6

ERRORS DETECTED: 0
LINKS GENERATED: 0
RUN-TIME: 18 SECONDS
3K CORE USED

PFUNCT 0370
PGETDA 2617
PGOTIT 1346
PNORDY 1771
PNTRDY 1765
PRDSEC 1105
PRTERP 0503
PTRVAG 2615
PUTSEC 0145
PUTTRK 0166
PYSRDY 1767
RCALOW 0060
RDERES 1275
RDSEC 0760
R0STAT 1224
READ 2167
READOK 0706
RECAL 0035
RECAL1 0034
RFINTQ 0355
ROT 1251
ROT3 2736
SAWIND 2714
SECHLF 0543
SECPL9 2124
SELFER 0620
SPBACK 2662
STASH 0437
STDLY 2654
STDONE 1031
STEPHO 2100
STPOUT 0275
SHGATF 0407
TEST 2352
TEST1 1351
TEST2 1350
TESTDN 1372
TIMERR 1667
TKSKER 2542
TRKEO 0246
TRYAGN 1413
TSTAGN 1353
TSTG0 2443
TSTRTN 0004
UDIF 0134
UNRDY 2767
UONE 0120
USAME 0141
UZERO 0127
WAIT 0743
WAITRN 2312
WATDAT 2021

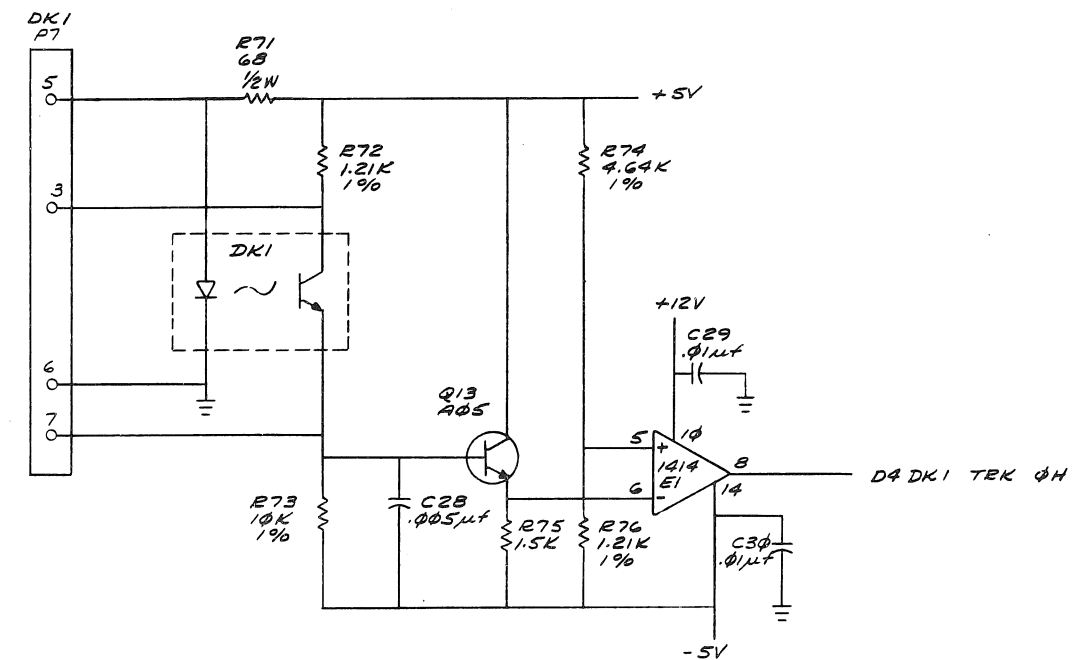
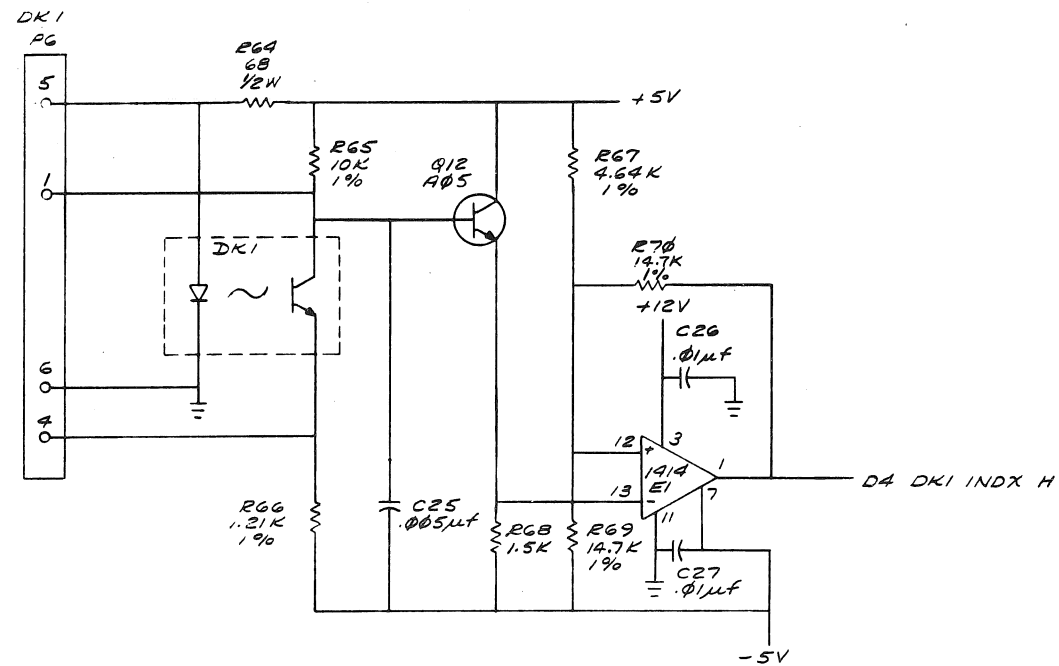
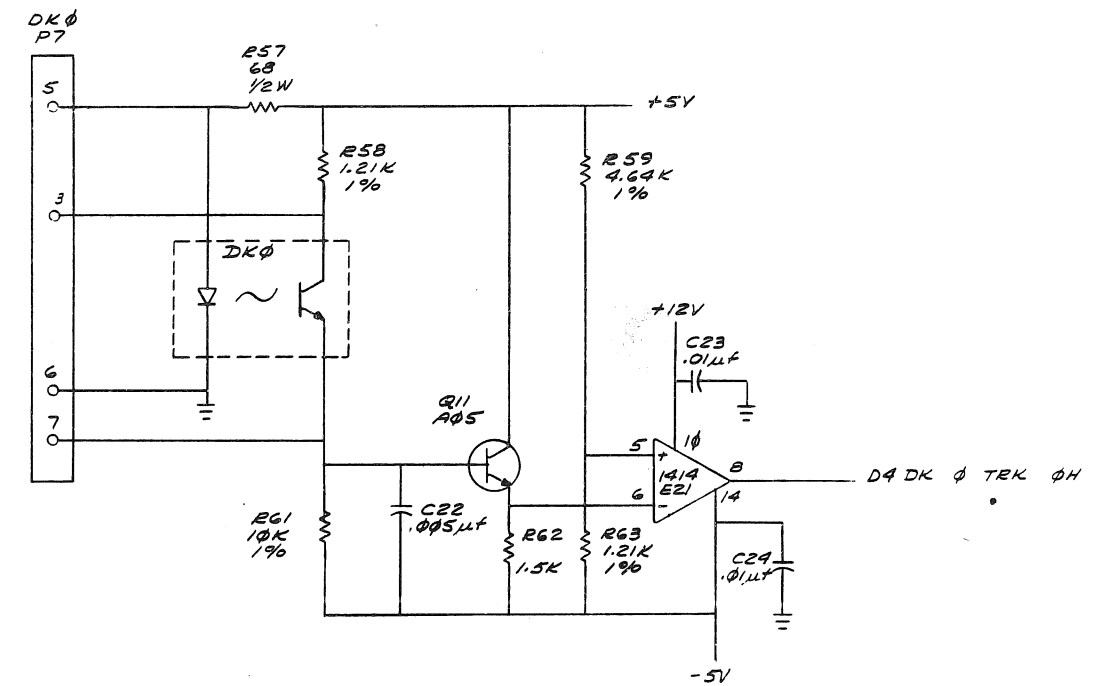
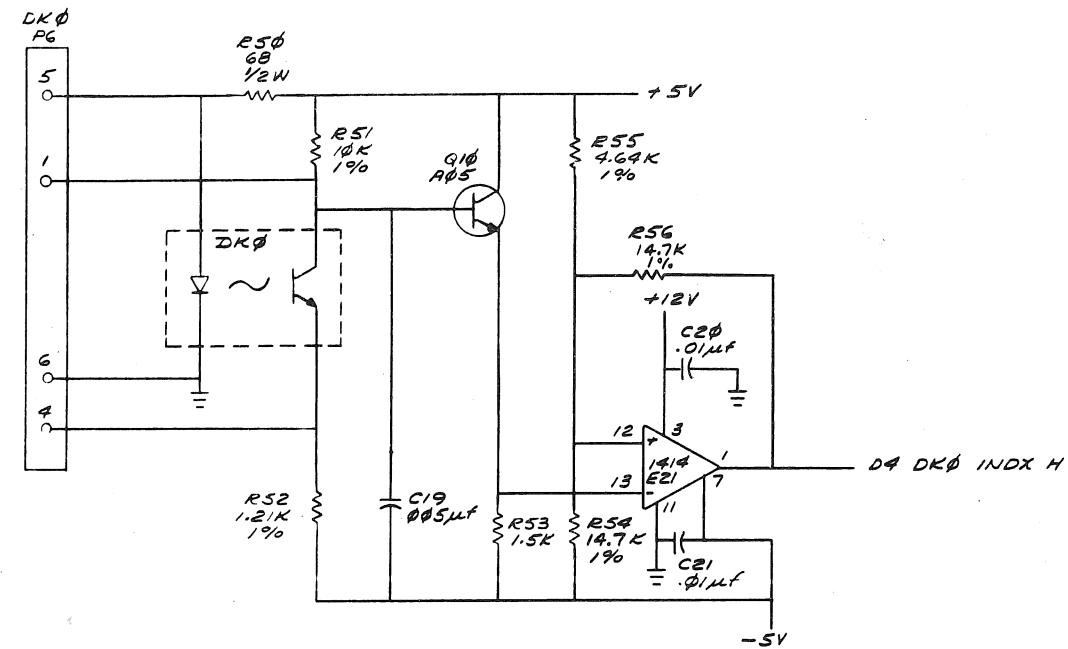
1. UNLESS OTHERWISE SPECIFIED:
 - A. ALL RESISTORS ARE 1/4W, $\pm 5\%$.
2. WASHER TO BE USED BETWEEN ITEMS 57 AND 58 WILL BE SUPPLIED WITH THE D44CB TRANSISTOR ONLY BY G.E.
THE WASHER IS ONLY REQUIRED WHEN USING THE G.E. TYPE TRANSISTOR.



7473	11	4
75451	4	B
74157	8	16
75452	4	8
74129	8	16
IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		
IC PIN LOCATIONS		

QTY		REF. DESIGNATION		DESCRIPTION		PART NO.		ITEM NO.	
FIRST USED ON OPTION MODEL				PARTS LIST					
M7727				ETCH BOARD REV. B					
				DRN. <i>[Signature]</i> DATE 12/31/74 CHG'D. <i>[Signature]</i> DATE 1/24/75 ENG. <i>[Signature]</i> DATE 1-24-75 PROJ. ENG. <i>[Signature]</i> DATE 1/24/75 <i>[Signature]</i> DATE 1/24/75 TITLE READ/WRITE CONTROL					
				NEXT HIGHER ASSY + +					
DEC NO.		EIA NO.		DEC NO.		EIA NO.		SCALE $\frac{1}{2}$ OF 6 SHEET 1 OF 6	
SEMICONDUCTOR CONVERSION CHART									

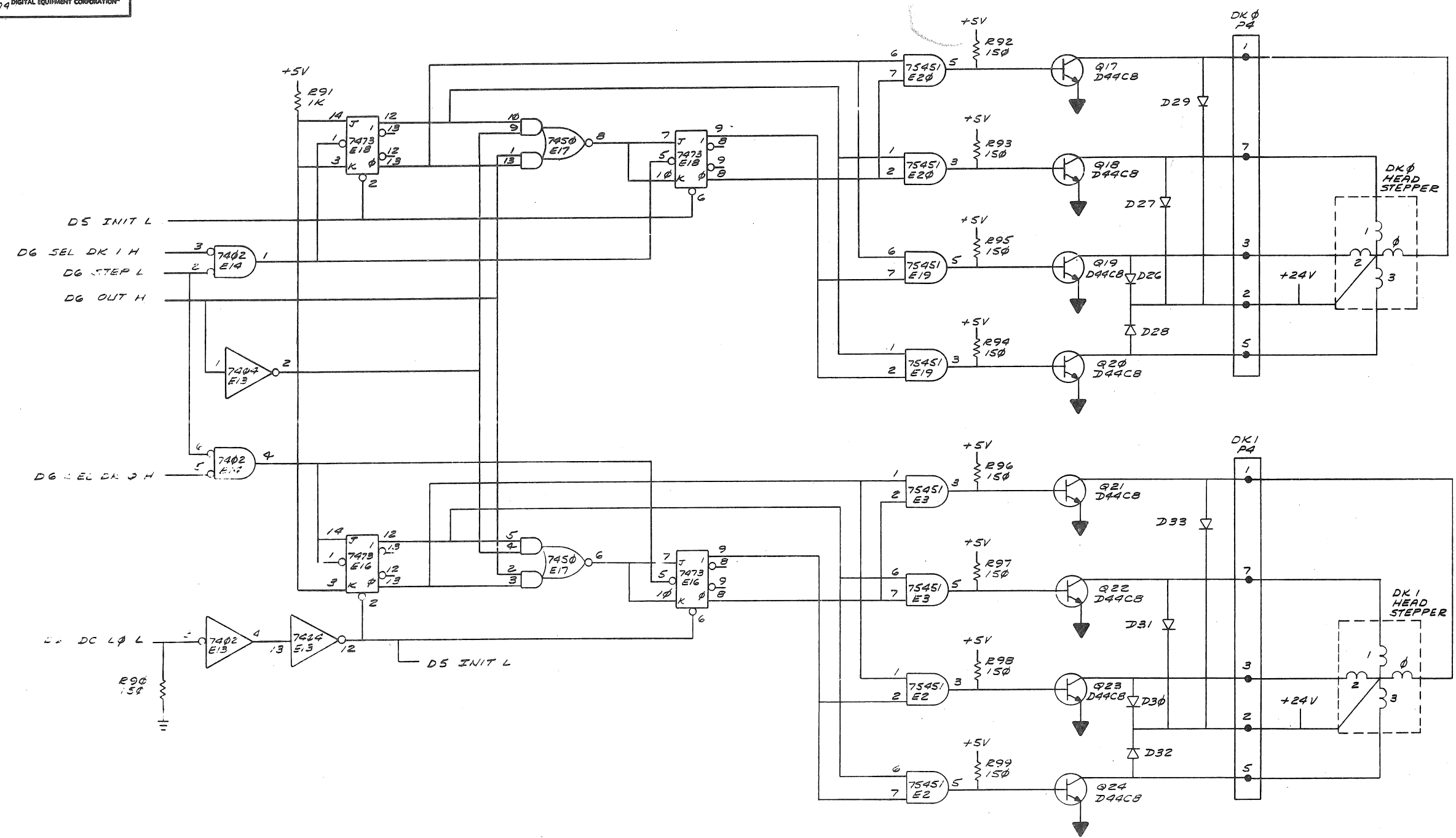
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
READ / WRITE CONTROL (D4)		DCS	M7727-0-1	C
SCALE		SHEET 4 OF 6	DIST.	

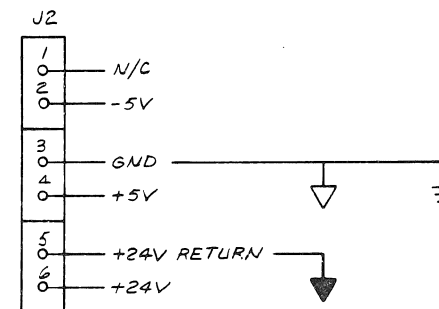
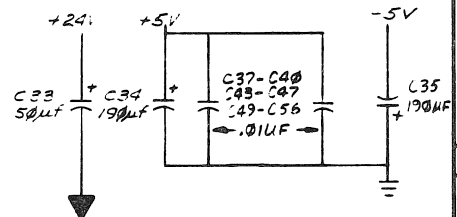
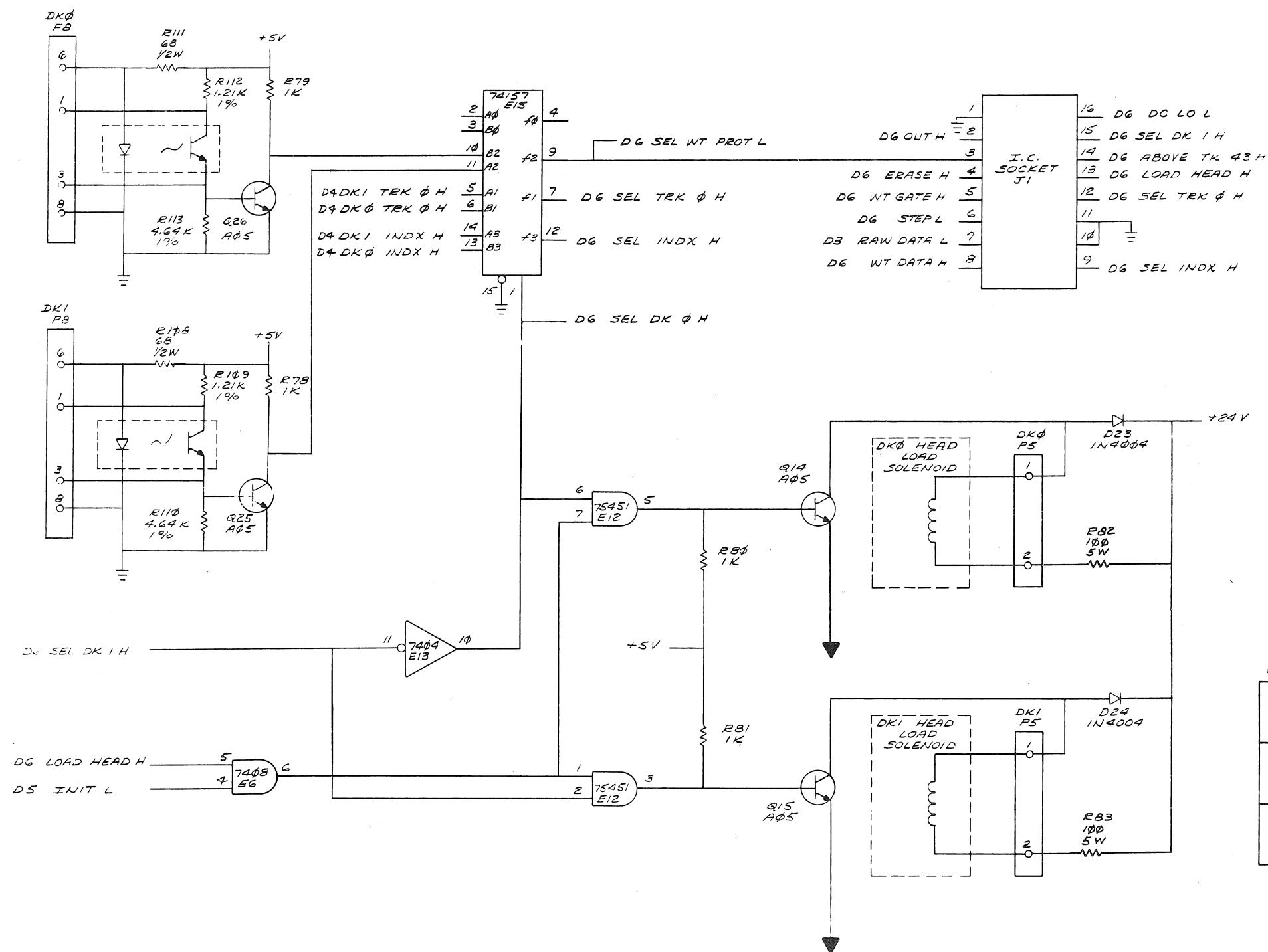
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REVISIONS		
CHK	CHANGE NO.	REV.

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1-0-2777W SCS 2



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE READ / WRITE CONTROL (D6)		SIZE CODE DCS		NUMBER M7727-0-1		REV. C
SCALE	SHEET 6 OF 6	DIST.				

THIS IS PRINT SET

--	--	--	--

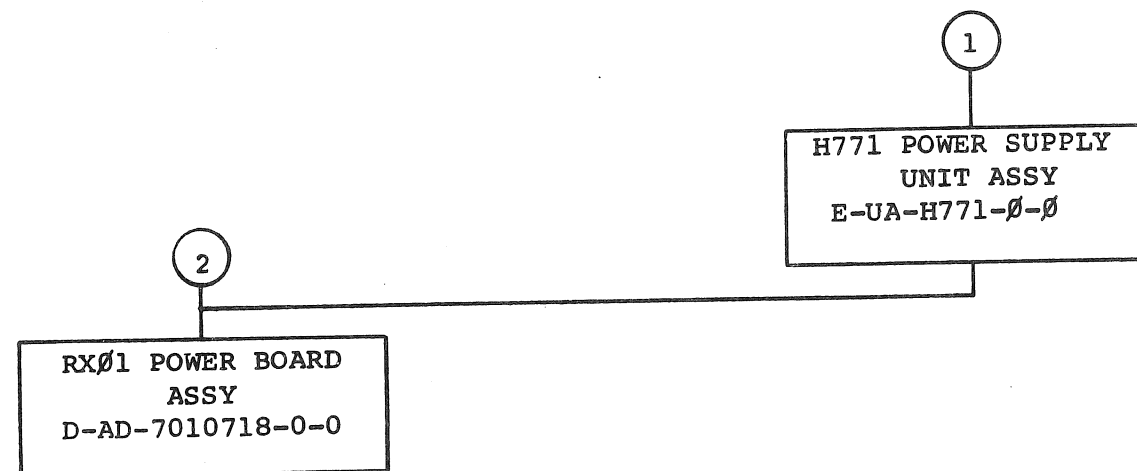
SEQUENCE

B-DD-H771-Ø
D-CS-H771-A-1
D-CS-H771-C-1
D-CS-H771-D-1
D-AD-7010718-0-0
D-CS-5411398-0-1

[illegible]

REVISIONS			
DATE	CHG. NO.	REV	
7-75	H771-1	A	
10-75	H771-2	B	
11-75	H771-3	C	
3-76	H771-4	D	

USED ON OPTION/MODEL		DRN. W. McCarthy	DATE 2/3/75	TITLE H771 POWER SUPPLY									
RXØ1		CHK'D. W.F.M.C. <i>dy</i>	DATE 6/13/75										
		PROJ. ENG. <i>dy</i>	DATE 6/13/75										
		PROD. <i>dy</i>	DATE 6/13/75	SIZE	CODE	NUMBER					REV		
		FIELD SERV. <i>dy</i>	DATE 6/13/75	B	DD	H771-Ø					D		
SHEET 1	OF 3			DIST									

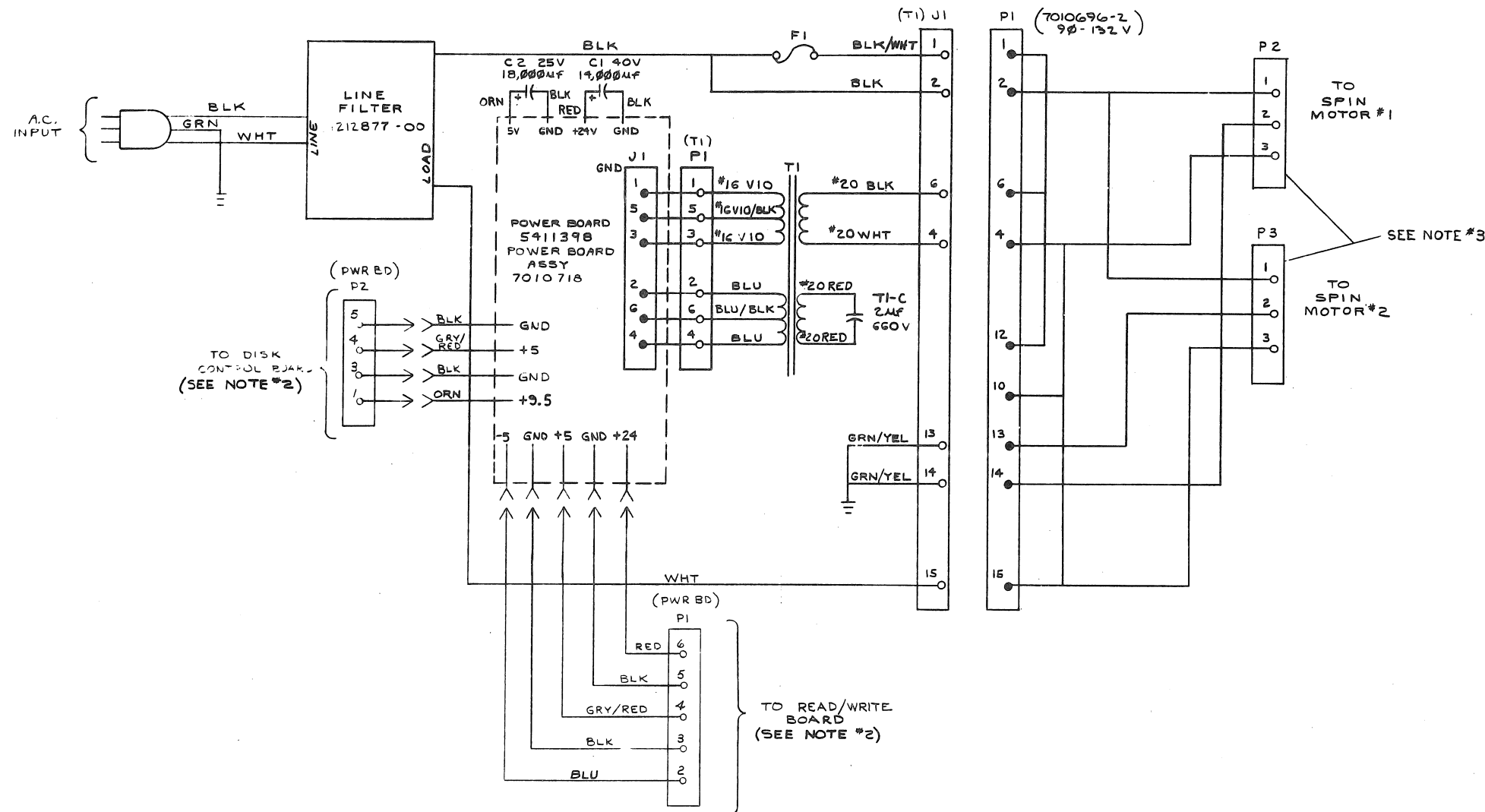


TITLE		SIZE	CODE	NUMBER	REV
H771 POWER SUPPLY	SHEET 2 OF 3	B	DD	H771-Ø	D

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NOTES:

1. ALL WIRE TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.
2. SLOT BETWEEN P1-4 + P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 + P2-5 ALSO CONTAINS A DUMMY PIN.
3. NO DOUBLE CRIMPS ARE ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).

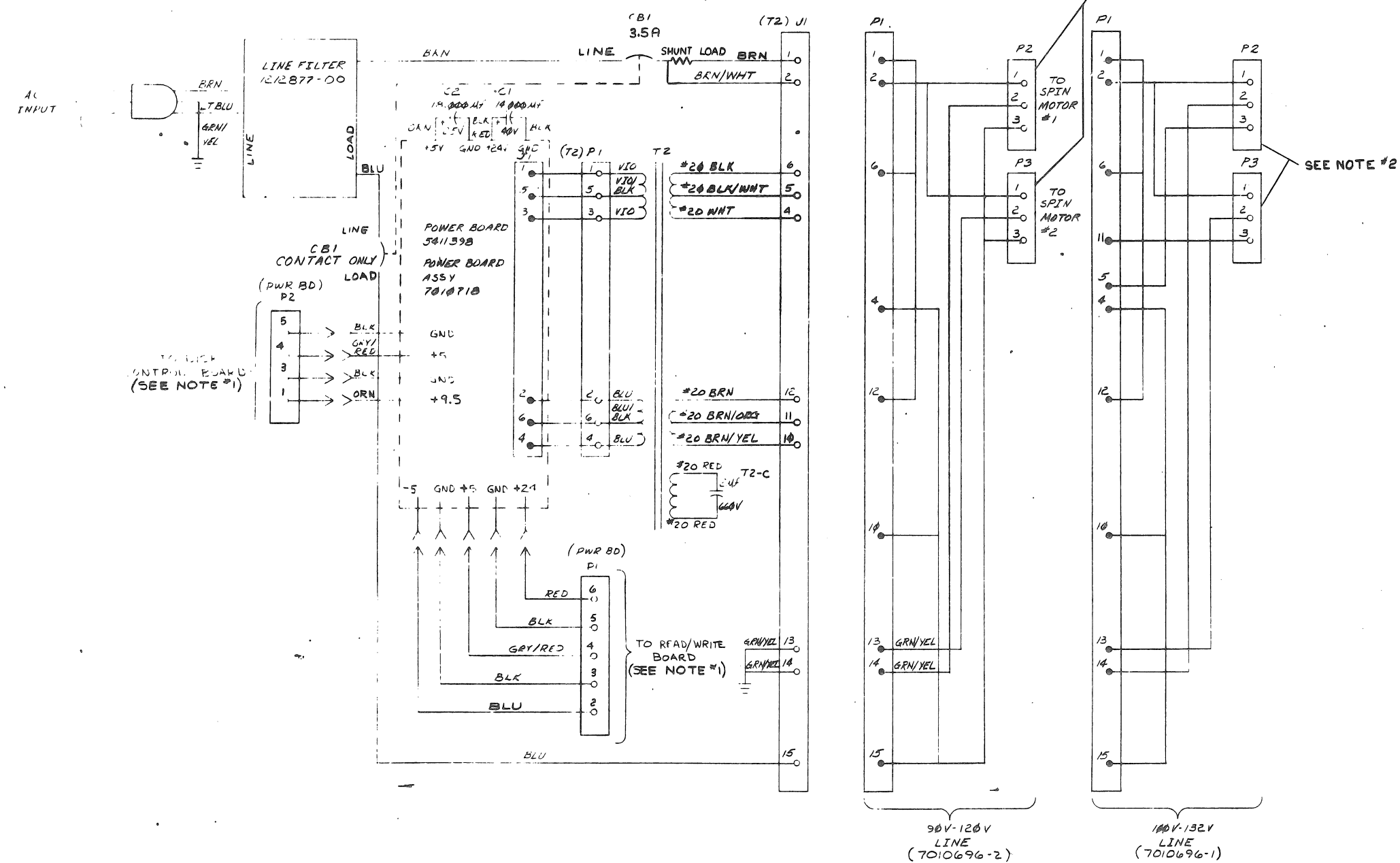


REVISIONS		
CHK#	CHANGE NO.	REV.
1	H771-000	A
B HAZE		
C HAZE		
D HAZE		
E HAZE		
F HAZE		
G HAZE		
H HAZE		
I HAZE		
J HAZE		
K HAZE		
L HAZE		
M HAZE		
N HAZE		
O HAZE		
P HAZE		
Q HAZE		
R HAZE		
S HAZE		
T HAZE		
U HAZE		
V HAZE		
W HAZE		
X HAZE		
Y HAZE		
Z HAZE		

DRN. <i>D.C. Olson</i>	<i>1/22/75</i>	FIRST USED ON	<i>Rx01</i>	digital	
CHK'D <i>WFM</i>	<i>2/6/75</i>	TITLE			
ENG. <i>Bull</i>	<i>2-10-75</i>	H771-A POWER CONNECTIONS			
PROJ. ENG. <i>WFM</i>	<i>2-10-75</i>				
PROD. <i>WFM</i>	<i>2/10/75</i>				
NEXT HIGHER ASSY.					
B-DD-H771-0		SIZE	CODE	NUMBER	REV.
SCALE NONE		D	CS	H 771-A-1	B
SHEET		DIST.			
OF					

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- NOTES:
1. SLOT BETWEEN PI-4 AND PI-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
 2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).
 3. ALL WIRES TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.

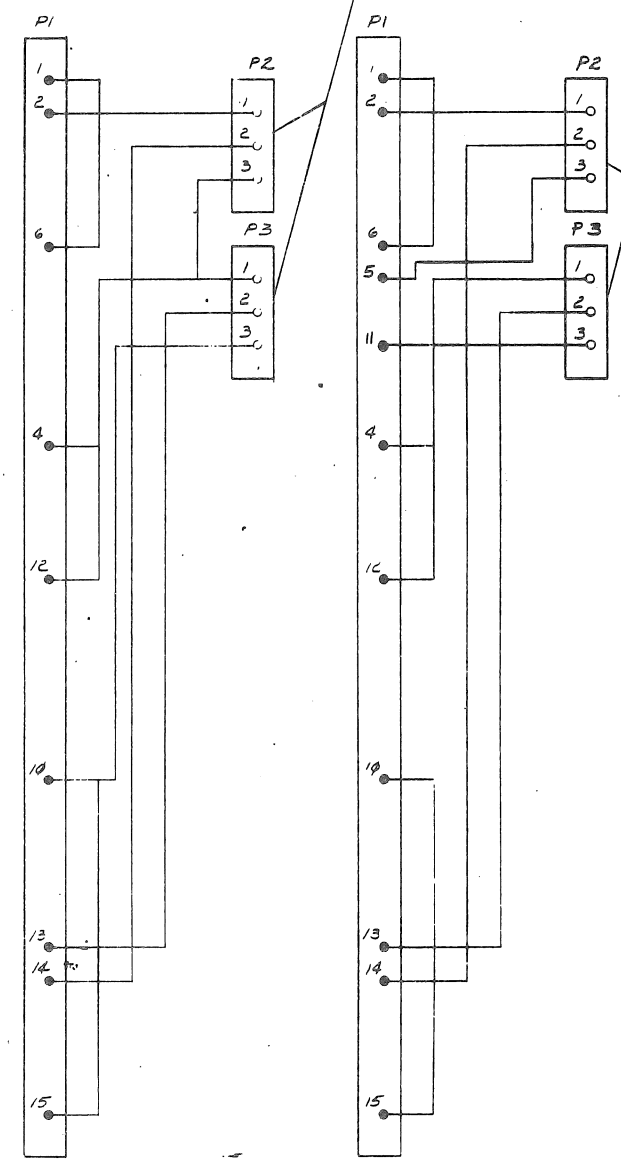
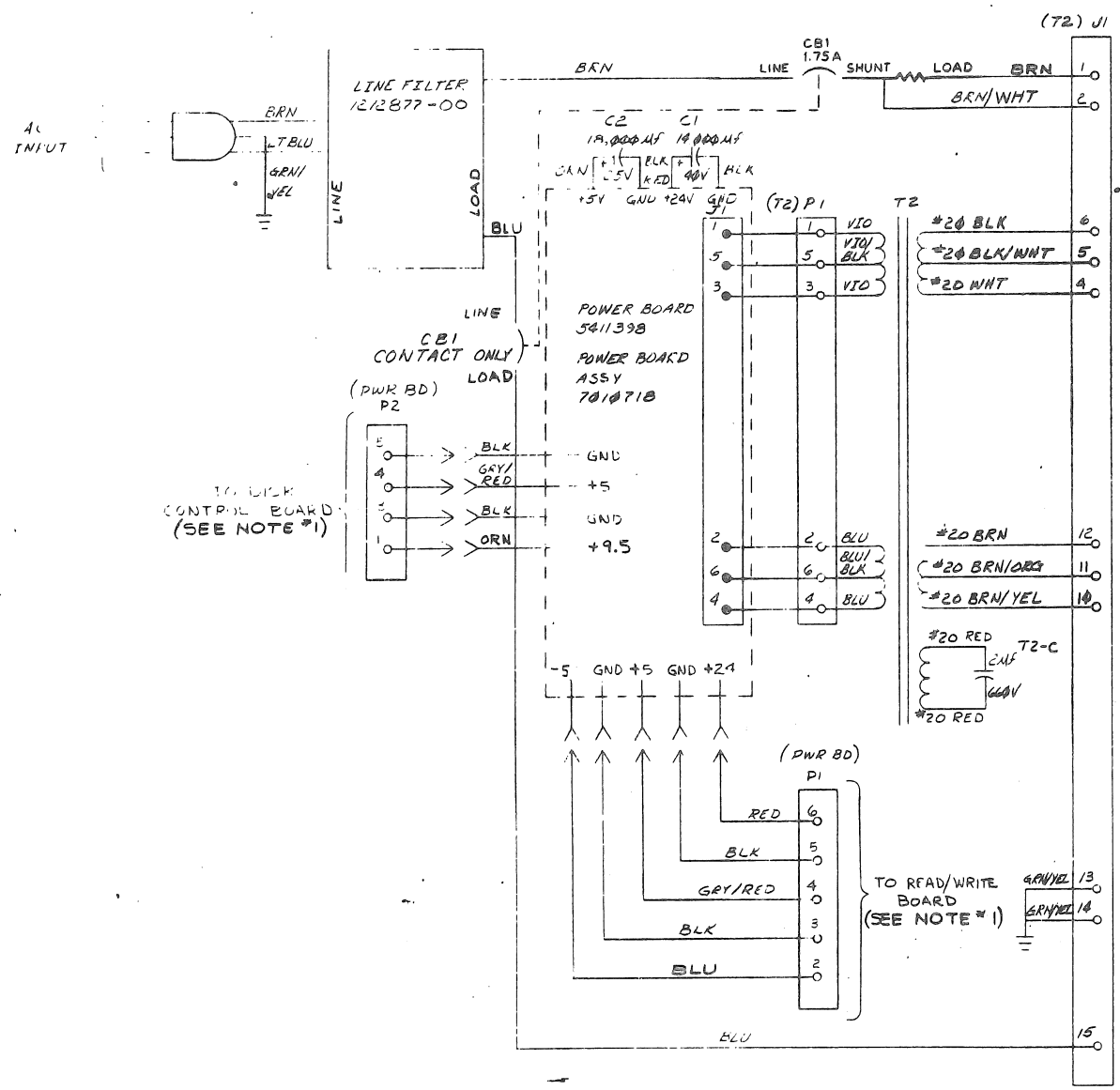


REV.	DATE	BY	CHKD	APPD
1	10/1/75	B. HAZEN		
2	10/1/75	B. HAZEN		
3	10/1/75	B. HAZEN		
4	10/1/75	B. HAZEN		
5	10/1/75	B. HAZEN		
6	10/1/75	B. HAZEN		
7	10/1/75	B. HAZEN		
8	10/1/75	B. HAZEN		

DRN. 101	FIRST USED ON 8-5-75	RX01
CHKD E. RENOLD	ENG. 10/1/75	PROJ. ENG. 10/1/75
PROD. 10/1/75		
NEXT HIGHER ASSY.		
B-DD-H77-C	SIZE CODE D	CS H77-C-1
SCALE	SHEET 1 OF 1	DIST.

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- NOTES:
1. SLOT BETWEEN PI-4 AND PI-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
 2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTORS TO MOTOR(S).
 3. ALL WIRES TO BE #18AWG UNLESS OTHERWISE SPECIFIED.



180V-240V LINE (7010696-4)

200V-264V LINE (7010696-3)

REV.	CHANGE NO.	DATE	BY	CHK'D
1	1	12-15-75	B. HAZEN	
2	2	12-15-75	B. HAZEN	
3	3	12-15-75	B. HAZEN	
4	4	12-15-75	B. HAZEN	
5	5	12-15-75	B. HAZEN	
6	6	12-15-75	B. HAZEN	
7	7	12-15-75	B. HAZEN	
8	8	12-15-75	B. HAZEN	

DRN	7-1-75	FIRST USED ON	RX0
CHK'D	12-15-75	TITLE	H771-D POWER CONNECTIONS
ENG.	12-15-75	PROJ. ENG.	12-15-75
PROD.	12-15-75	PROD.	12-15-75
NEXT HIGHER ASSY.		SIZE	D
B-DD-H771-0		CODE	CS
SCALE		NUMBER	H771-D-1
SHEET	1 OF 1	DIST.	

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P4
SOLDER TO
COMPONENT
SIDE OF
BOARD

SOLDER TO COMPONENT
SIDE OF BOARD
P5

P6
SOLDER TO COMPONENT
SIDE OF BOARD

10.44
REF

SEE NOTE 3

PWR BD
(COMPONENT SIDE SHOWN)

4.75
REF

POINT 4

POINT 3

POINT 2

POINT 1

P3
SOLDER TO COMPONENT
SIDE OF BOARD

7 (QTY 4)

POINT 5

POINT 4

POINT 3

POINT 2

POINT 1

P2
SOLDER TO FAR SIDE OF BOARD

P1
SOLDER TO FAR SIDE
OF BOARD

WIRE TABLE

ITEM NO.	DESCRIPTION	FROM		TO		LENGTH
		AWG	COLOR	CONN	TERM	
1	18 BLU			P1 POINT 1	PWR #11 SOLDER	
	BLK			P1 POINT 2	PWR #6	
	GRY/RED			P1 POINT 3	PWR #9	
	BLK			P1 POINT 4	PWR #5	
	RED			P1 POINT 5	PWR #12	
2	ORN			P2 POINT 1	PWR #4	
	BLK			P2 POINT 2	PWR #7	
	GRY/RED			P2 POINT 3	PWR #10	
	18 BLK			P2 POINT 4	PWR #8	
3	14 RED			P3	ITEM 7 PWR #13	13 IN ±.25
4	14 BLK			P5	ITEM 7 PWR #2	7 IN ±.25
5	14 ORN			P4	ITEM 7 PWR #1	11 IN ±.25
4	14 BLK			P6	ITEM 7 PWR #3 SOLDER	9 IN ±.25

NOTES:

1. STRIP LENGTH FOR ITEMS 3, 4 & 5 ARE TO BE .16 LONG.
2. THE BLACK WIRES ON P1 & P2 CAN BE INTERCHANGED BETWEEN POINTS 5, 6, 7, & 8 ON THE POWER BOARD.
3. INK STAMP ASS'Y NO. 7010718 IN FIGURES, 13 HIGH WHERE SHOWN.

4 CONN, SOLDERLESS	9007928-00	7
1 POWER SUPPLY BOARD, RXØ1	D-05-5411398-0-1	6
1/8 WIRE, #14 AWG, IPVC, ORANGE	9107370-33	5
1/8 WIRE, #14 AWG, IPVC, BLACK	9107370-00	4
1/8 WIRE, #14 AWG, IPVC, RED	9107370-22	3
1 HARNESS, DISK CONTROL BOARD	D-1A-7010853-0-0	2
1 HARNESS, READ/WRITE BOARD	D-1A-7010854-0-0	1

DESCRIPTION		DWG./PART NO.		ITEM NO.	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES					
ANGLES ±0° 30'		NOMINAL DIMENSION RANGE INCHES			
SURFACE QUALITY IN	CLASS OF ACCURACY (CHECK ONE)	OVER 0 TO 0.2	OVER 0.2 TO 1.2	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0
		0.2	1.2	4.0	12.0
MICROINCHES	MEDIUM	±.004	±.008	±.012	±.016
	PREPARED	±.012	±.016	±.020	±.024

THIRD ANGLE PROJECTION	DRN. T. Quillen 1/24/75	FIRST USED ON	H771
REMOVE BURRS AND BREAK SHARP CORNERS	CHK'D M. C. 1/25/75	TITLE	RXØ1 POWER BOARD ASS'Y
DO NOT SCALE DWG	PROJ. ENG. 1/25/75	SIZE	E-UA-H771-0-0
MATERIAL SEE PARTS LIST	PROD. 1/25/75	SCALE	1/1
FINISH	NEXT HIGHER ASSY.	SHEET	1 OF 1
		DIST.	

REV. L
NUMBER 7010718-0
SIZE CODE D

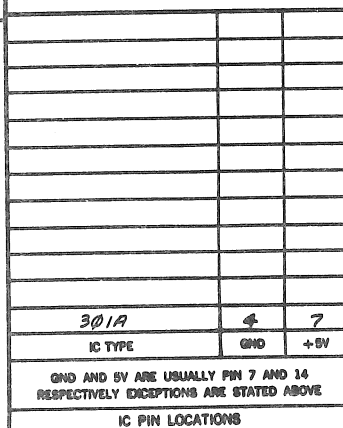
B

A

REV.	CHANGE NO.	DATE	BY	CHK
A	1	1/24/75	T. Quillen	
B	1	1/25/75	M. C.	
C	1	1/25/75	M. C.	
D	1	1/25/75	M. C.	
E	1	1/25/75	M. C.	
F	1	1/25/75	M. C.	
G	1	1/25/75	M. C.	
H	1	1/25/75	M. C.	
I	1	1/25/75	M. C.	
J	1	1/25/75	M. C.	
K	1	1/25/75	M. C.	
L	1	1/25/75	M. C.	
M	1	1/25/75	M. C.	
N	1	1/25/75	M. C.	
O	1	1/25/75	M. C.	
P	1	1/25/75	M. C.	
Q	1	1/25/75	M. C.	
R	1	1/25/75	M. C.	
S	1	1/25/75	M. C.	
T	1	1/25/75	M. C.	
U	1	1/25/75	M. C.	
V	1	1/25/75	M. C.	
W	1	1/25/75	M. C.	
X	1	1/25/75	M. C.	
Y	1	1/25/75	M. C.	
Z	1	1/25/75	M. C.	

DEC FORM NO.
ORD 100-C

1. UNLESS OTHERWISE SPECIFIED
A. ALL RESISTORS ARE 1/4W, ±5%.
2. DOTTED AREAS COMPONENT NOT ON BOARD.
3. AT TIME OF MODULE ASSY, ITEM 49 SHOULD
BE APPLIED BENEATH Q2, Q3 & Q5.
4. AT TIME OF ASSEMBLY, Q2, Q3 AND Q5 MOUNTING
HARDWARE MUST BE TORQUED TO 4 TO 6 INCH POUNDS.
5. Q4, Q6 AND Q7 OUTLINES CORRESPOND TO GENERAL
ELECTRIC TYPE TRANSISTORS.
6. FLAT RECTANGULAR WASHER SUPPLIED BY VENDOR
TO BE MOUNTED UNDER Q2 AND Q5. SCREWHEAD.



REF	X-Y COORDINATE	HOLE LOCATION	K-CO-5411398-0-A	
DEF	ASSY/DEILLING HOLE LAYOUT	D-AH-5411398-0-5		2
DEF	MODULE ECO HISTORY	B-MH-5411398-0-6		3
1	ETCHED CIRCUIT BOARD	5011397-0-0		4
3 C5, C6, C7	CAP .01 uF 100V 20% DISC	1001610-01		5
2 C5, C8	CAP 1000 uF 16V ELEC	1011849-02		6
3 C6, C10, C11	CAP .1 uF 100V 20% DISC.	1000930-00		7
1 C9	CAP 190 uF 12V 10% ELEC	1009433-00		8
2 D1, D2	DIODE A158 (N5624)	1110420-00		9
2 D3, D4	DIODE ME752	1110615-00		10
1 D5	DIODE IN4744 15V 10%	1105648-00		11
				12
2 D7, D6	DIODE 5ZT10910 5.1V 2%	1110713-00		13
1 D8	DIODE D664	1100114-00		14
2 D9, D10	DIODE IN4004	1105796-00		15
1 D11	DIODE INTS4A 6.8V 5%	1109991-00		16
2 R5, R17	RES 39 1/4W 5% CC	1302377-00		17
1 R6	RES 470 1/4W 5% CC	1300316-00		18
1 R7	RES .08 5W 3% CC	1311603-00		19
1 R8	RES 47 1/4W 5% CC	1300302-00		20
1 R9	RES 1M 1/4W 5% CC	1309595-00		21
1 R12	RES 270 2W 5% CC	1305380-00		22
1 R13	RES 511 3/4W 1% CC	1300324-00		23
1 R14	RES 10 2W 10% CC	1300172-00		24
1 R15	RES 180 1W 5% CC	1300262-00		25
1 R16	RES 10 1/4W 5% CC	1301317-00		26
				27
1 R18	RES 120 1/4W 5% CC	1300247-00		28
2 R19, R20	RES 1K 1/4W 5% CC	1300365-00		29
1 R22	RES 220 1/4W 5% CC	1300271-00		30
1 R21	RES 120 1W 5% CC	1301838-00		31
1	HEAT SINK	1212201-00		32
1 Q1	TRANS DEC 2219-2	1501883-00		33
1 Q2	TRANS D44C3	1510171-01		34
1 Q3	TRANS DEC3715	1503068-00		35
2 Q4, Q6	TRANS MXA A05	1510705-00		36
1 Q5	TRANS D4SH3	1510708-01		37
1 Q7	TRANS MXA A53	1510706-00		38
1 E1	I.C. DEC 301AN	1910282-00		39
4	EYELET	3007836-00		40
2	TERMINAL LUG, SOLDER	9009676-00		41
1 J1	CONNECTOR 6 PIN	1211342-0 6		42
				43
1 R4	RES 560 1/4W 5% CC	1301830-01		44
1 R23	RES 75 1W 5% CC	1305281-00		45
3 R1, R10, R11	RES 10K 1/4W 5% CC	1300479-00		46
1 R2	RES 390 2W 5% CC	1301864-00		47
1 R3	RES 620 1/4W 5% CC	1303178-00		48
AIR	THERMAL COMPOUND	9008268-00		49
2	SCREW 4-40 X 1/2	9006013-04		50
5	KEPNUT 4-40	9006357-00		51
5	WASHER FLAT 4-40	9006655-00		52
				53
1	SCREW 4-40 X 5/16 (PHILLIPS HD)	9006011-1		54
1	SCREW 4-40 X 7/16	9006012-04		55
1	SCREW 4-40 X 1/2 (PHILLIPS HD)	9006013-1		56

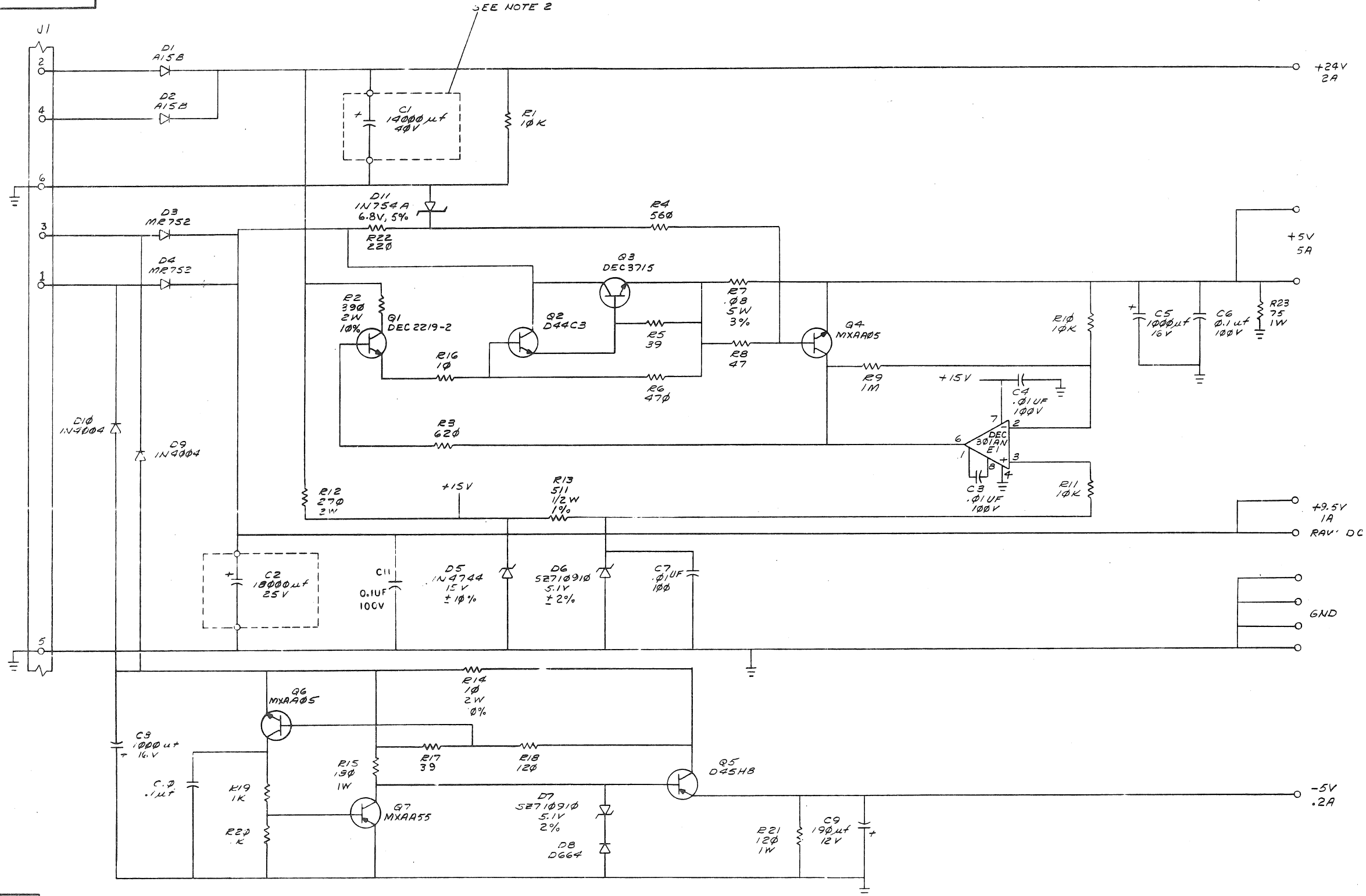
QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST				

ETCH BOARD REV.			
	D		

DRN. CHKD. ENG. PROJ. ENGR. DATE NEXT HIGHER ASSY	DATE DATE DATE DATE DATE	RXOI POWER SUPPLY
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DEC NO.	EIA NO.	SIZE CODE	NUMBER	REV.
		D CS	5411398-0-1	C

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REVISIONS		
CHK	CHANGE NO.	REV.



THIS IS PRINT SET

SEQUENCE

UNIT VARIATIONS

PRINT SET

TITL

7013503-0	COOLING UNIT FOR DUAL RX01 115V
7013503-1	COOLING UNIT FOR DUAL RX01 230V
7013503-2	COOLING UNIT FOR SINGLE RX01 115V
7013503-3	COOLING UNIT FOR SINGLE RX01 230V
7013503-4	7013503-0 W/O PACKAGING
7013503-5	7013503-1 W/O PACKAGING
7013503-6	7013503-2 W/O PACKAGING
7013503-7	7013503-3 W/O PACKAGING

[illegible][illegible]

