

Pinout Connections for LABPAK

Port 1

Pin	Signal	Comment
1	Timer0 Gate	Normally pulled high to enable timer
14	Timer0 Out	The output from the timer
2	2 Mhz Out	Also input to Timer0 - Rising edge
15	Timer1 Gate	as above
3	Timer1 Out	
16	Timer1 In	Input to the timer - Rising edge
4	Timer2 Gate	
17	Timer2 Out	
5	Timer2 In	
18	Pacer Gate	Is pulled high internally. Take low to disable
6	Ground	Digital ground
19	Trig0	
7	Clk0	
20	Trig1	
8	Clk1	
21	NC	
9	Schmitt out	High true output of schmitt trigger
22	Aux Lamp	Lamp on front panel. +5V to illuminate.
10	Schmitt in	Analog converter trig input
23	Threshold	Sets trig level for above. Default is TTL compatable.
11	Slope	High level (def) to trig ADC on falling edge of Schmitt
24	Ground	Analog ground
12	+5Volt	Caution do not short.
25	+15Volts	"
13	-15Volts	"

Port 2 Connections

Pin	Signal	Comment
1	Gnd	Analog Ground
14	Chan0	Analog input
2	Chan8	" " mates with Chan0 for Diff mode
15	Chan1	
3	Gnd	
16	Chan9	mates with Chan1 for Diff mode
4	Gnd	
17	Chan2	
5	Chan10	mates with Chan2 for Diff mode
18	Chan3	
6	Gnd	
19	Chan11	mates with Chan3 for Diff mode
7	Gnd	
8 20	Chan4	mates with Chan4 for Diff mode
21	Chan5	
9	Gnd	
22	Chan13	mates with Chan5 for Diff mode
10	Gnd	
23	Chan6	
11	Chan14	mates with Chan6 for Diff mode
24	Chan7	(Maint use also)
12	Gnd	
25	Chan15	mates with Chan7 for Diff mode
13	Gnd	No Connection

Port 3 - Port 6 Digital Input/Output

Pin	Signal	Comment
1	Gnd	Digital Ground
14	Pull up	220R pull up to +5Volts
2	Ready out	High indicates device has data or can receive data
15	Data 15	Most significant bit of data word
3	Strobe in	Rising edge strobes data in or out
16	Data 14	
4	Gnd	
17	Data 13	
5	Data 0	
18	Data 12	
6	Data 1	
19	Data 11	
7	Data 2	
20	Data 10	
8	Data 3	
21	Data 9	
9	Data 4	
22	Data 8	
10	Data 5	
23	Gnd	
11	Data 6	
24	Delay in	Input to a network which may be used to delay
12	Data 7	
25	Delay out	ready back in to strobe.
13	Gnd	

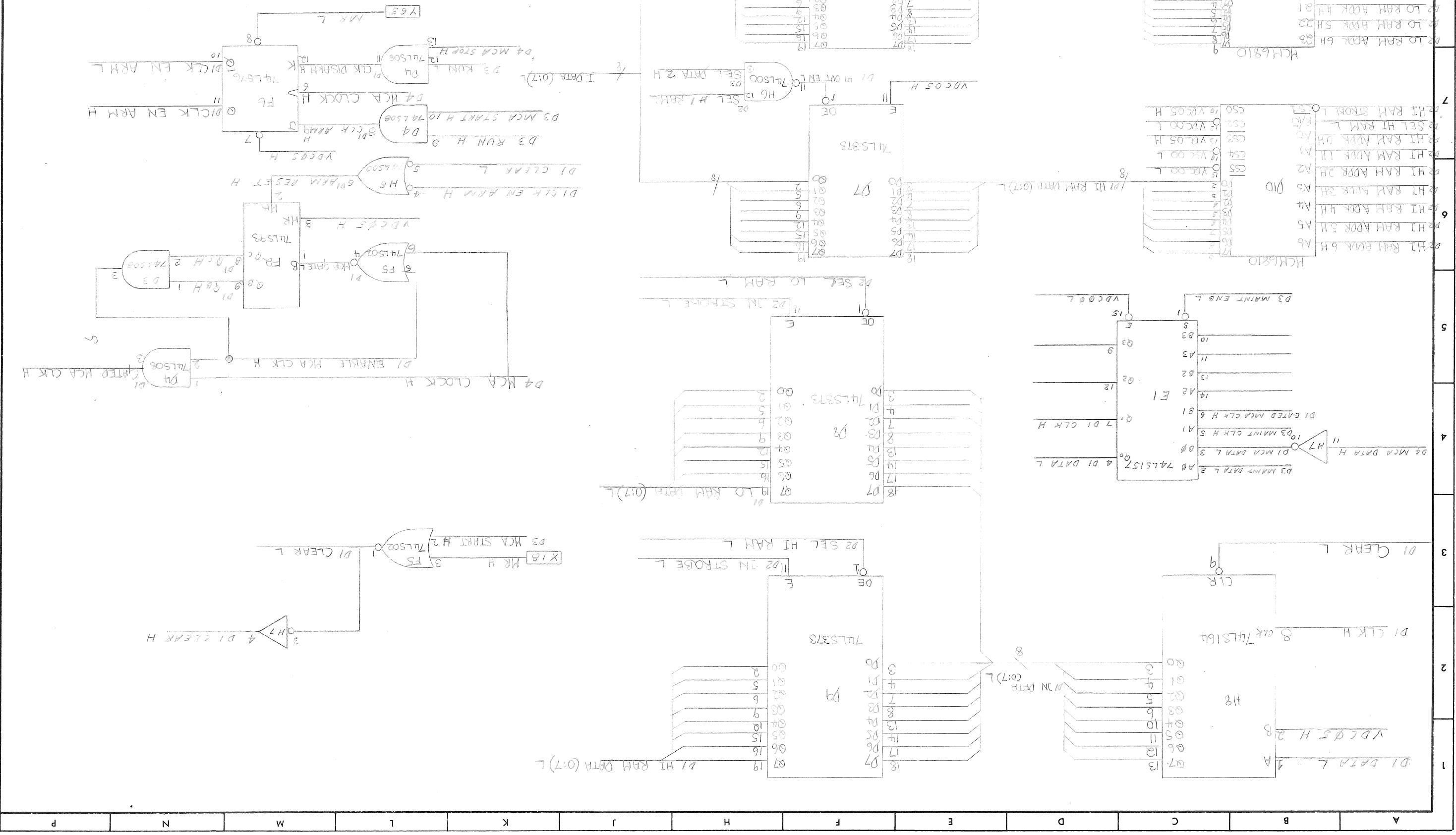
Port 7 Pin	Connections Signal	Analog output Comment
1	Dac0 out	Output from the first Digital to analog converter
14	Gnd	Analog ground
2	Dac1 out	
15	Gnd	
3	NC	
16	NC	
4	NC	
17	NC	
5	Rdyl out	Indicates Dac1 is ready for a new value
18	NC	
6	Stbl in	Strobes a new value into Dac1
19		All other pins have no connection at present
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Port	8	Connection	Serial Data
Pin		Signal	Comment
1		nc	
	14	nc	
2		Rx Data	
	15	nc	
3		Tx Data	
	16	nc	
4		RTS	Looped internally to pin 5
	17	nc	
5		CTS	
	18	nc	
6		DSR	Looped internally to pins 8 and 20
	19	nc	
7		Gnd	
	20	DTR	
8		Carrier	
	21		
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	22		
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	23		
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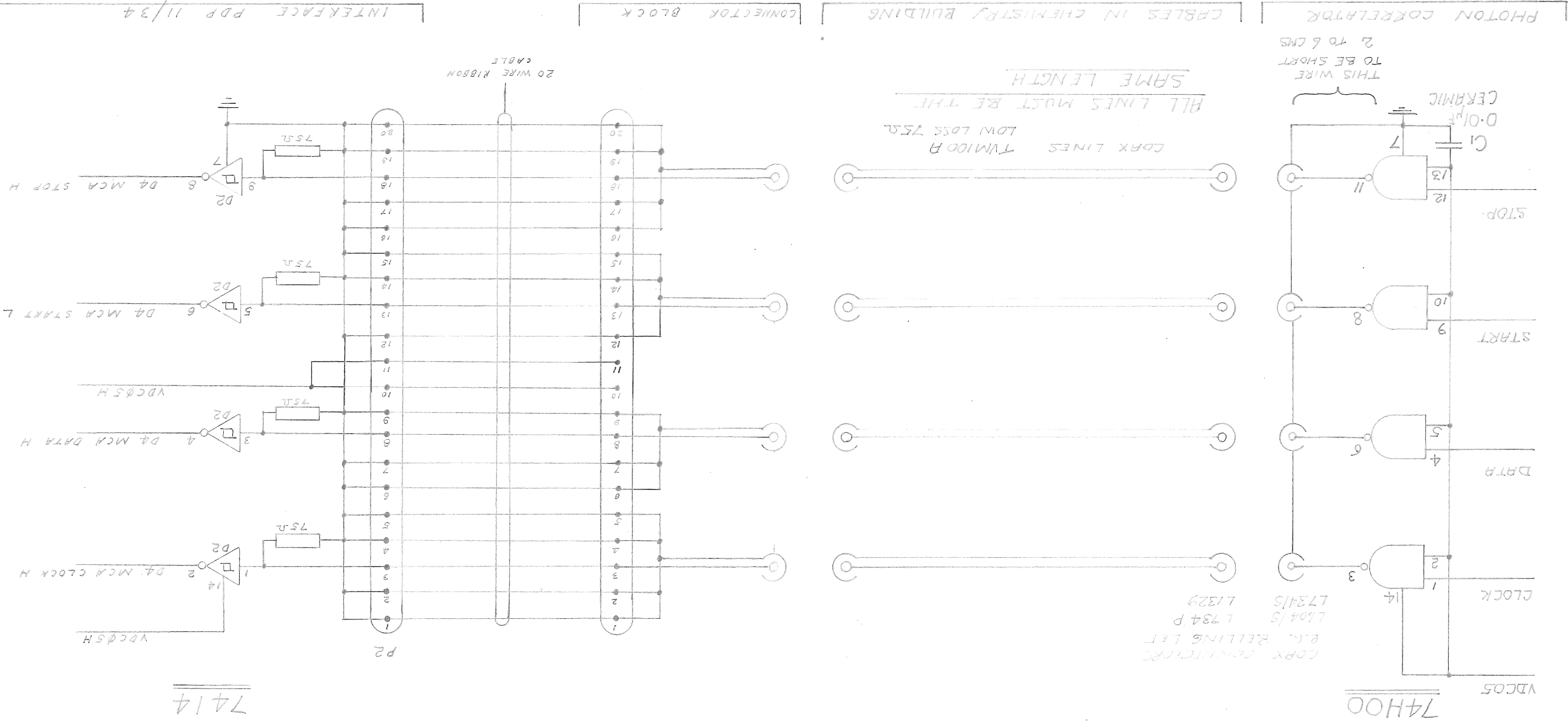
Terminal Pin	Port Connection Signal	Serial Data Comment
1	nc	
14	nc	
2	Rx Data	
15	nc	
3	Tx Data	
16	nc	
4	RTS	Looped internally to pin 5
17	nc	
5	CTS	
18	nc	
6	DSR	Looped internally to pins 8 and 20
19	nc	
7	Gnd	
20	DTR	
8	Carrier	
21		
9		
22		
10		
23		
11		
24		
12		
25		
13		

Comm Pin	Line Signal	Connection	Serial Data Comment
1	nc		
14	nc		
2	Tx Data		
15	nc		
3	Rx Data		
16	nc		
4	RTS		Looped internally to pin 5
17	nc		
5	CTS		
18	nc		
6	DSR		Looped internally to pins 8 and 20
19	nc		
7	Gnd		
20	DTR		
8	Carrier		
21			
9			
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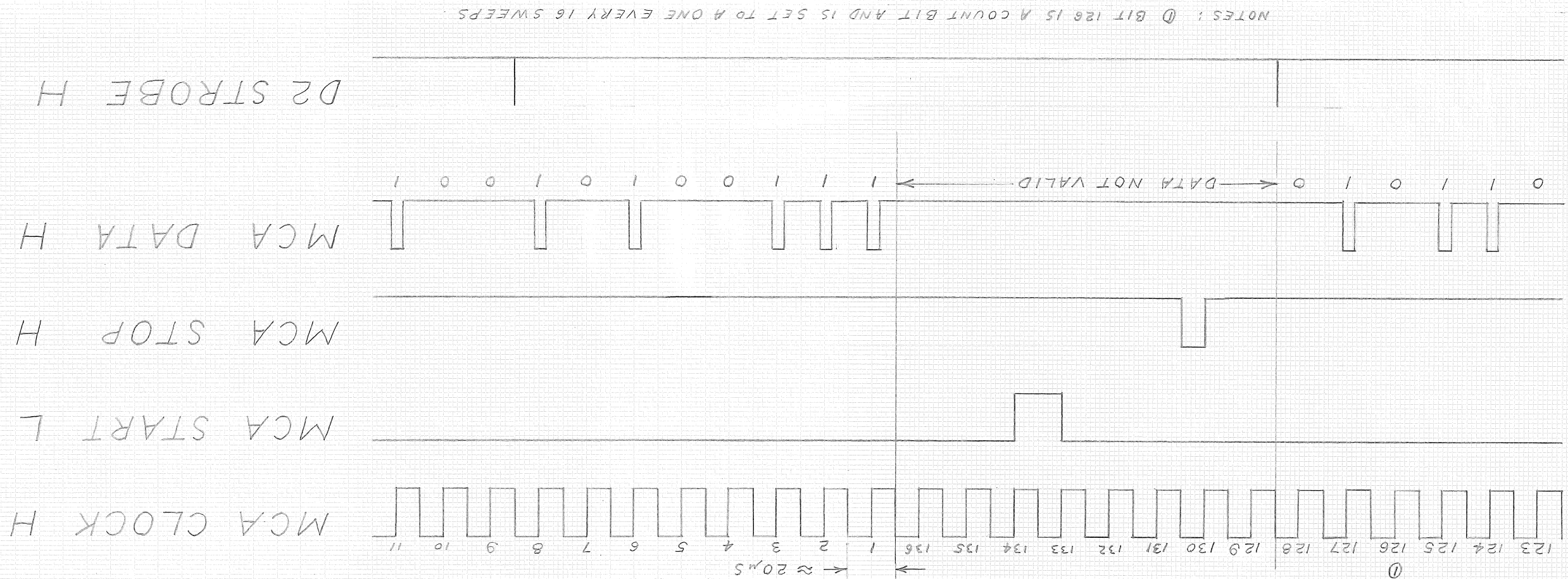
NOTE: 1. 74LS93 VCC = PIN 5, GND = PIN 10
2. HCH6810 VCC = PIN 34, GND = PIN 1



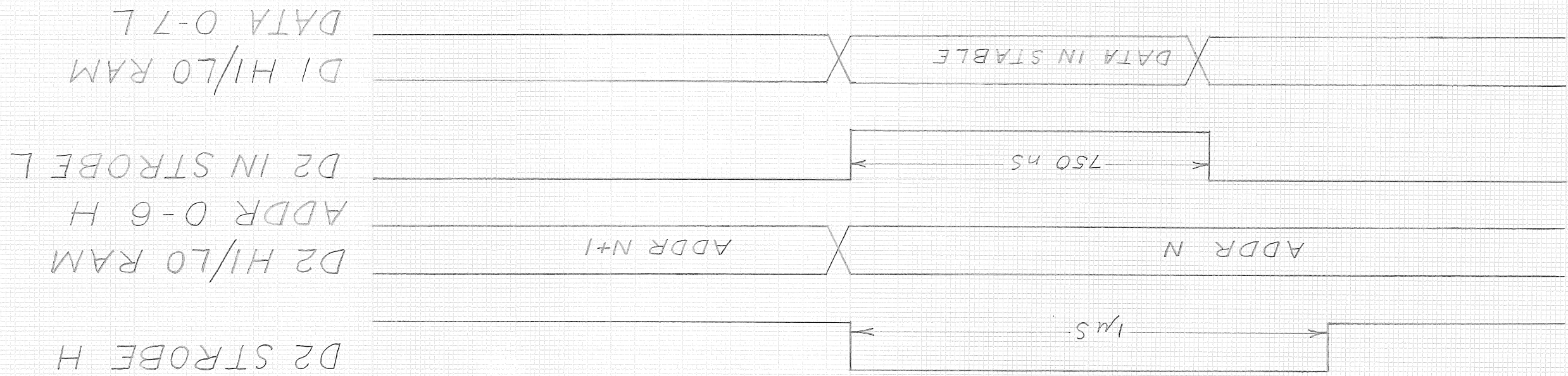
A	B	C	D	E	F	H	J	K	L	W	Z	P
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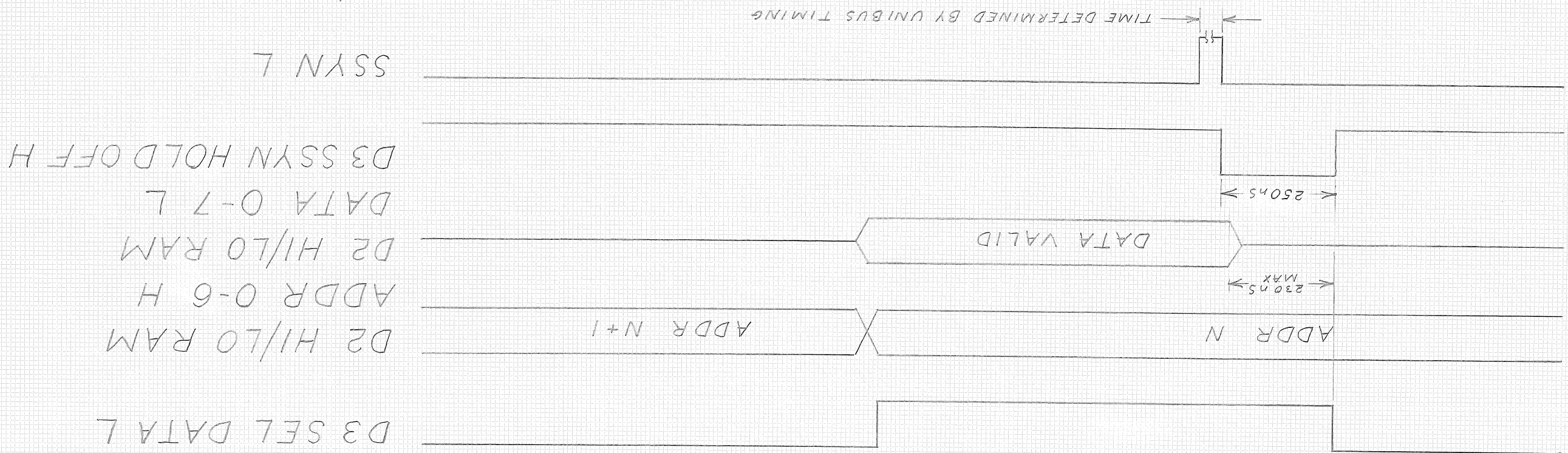
PHOTON CORRELATOR TIMING

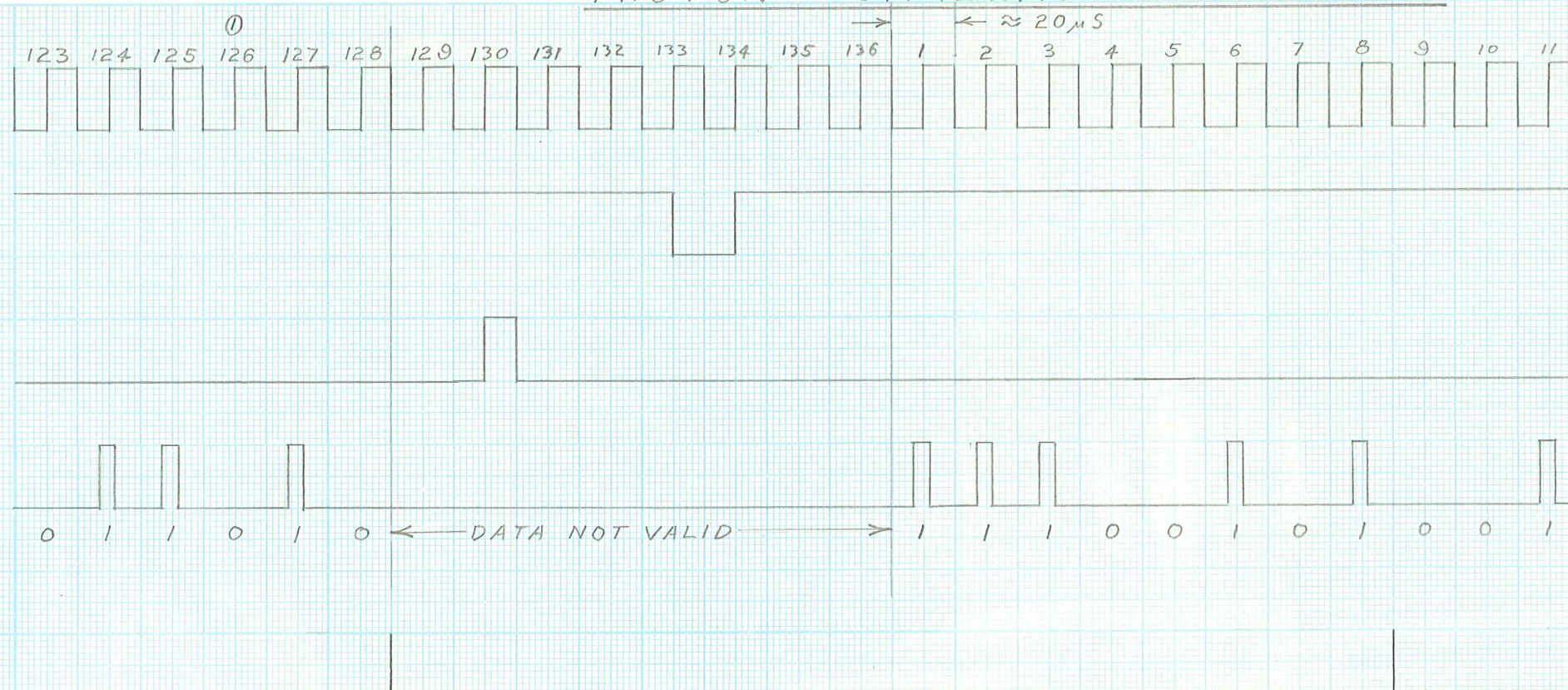


RAM WRITE CYCLE

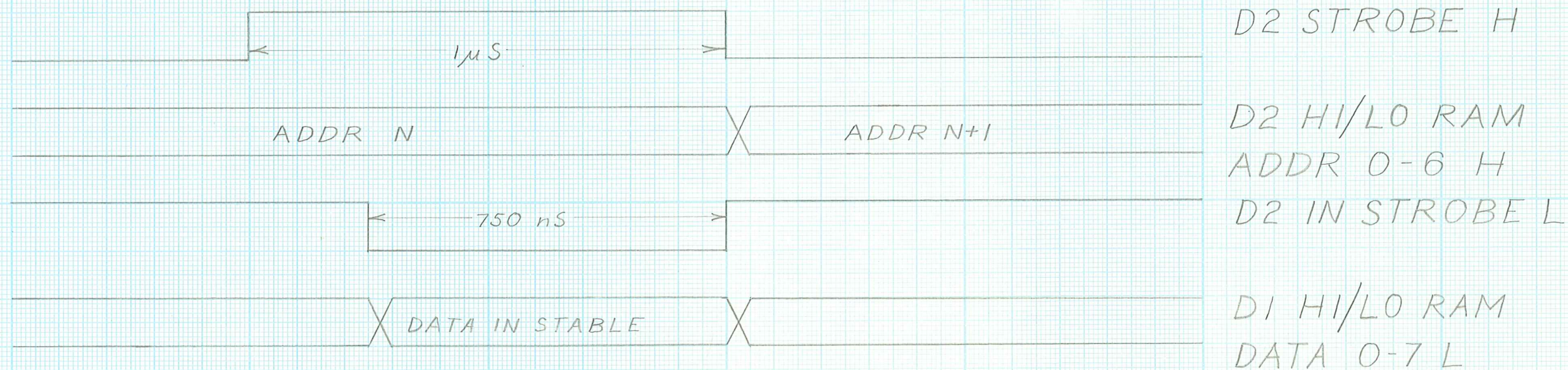


RAM READ CYCLE



PHOTON CORRELATOR TIMING

NOTES: ① BIT 126 IS A COUNT BIT AND IS SET TO A ONE EVERY 16 SWEEPS.

RAM WRITE CYCLE

RAM READ CYCLE