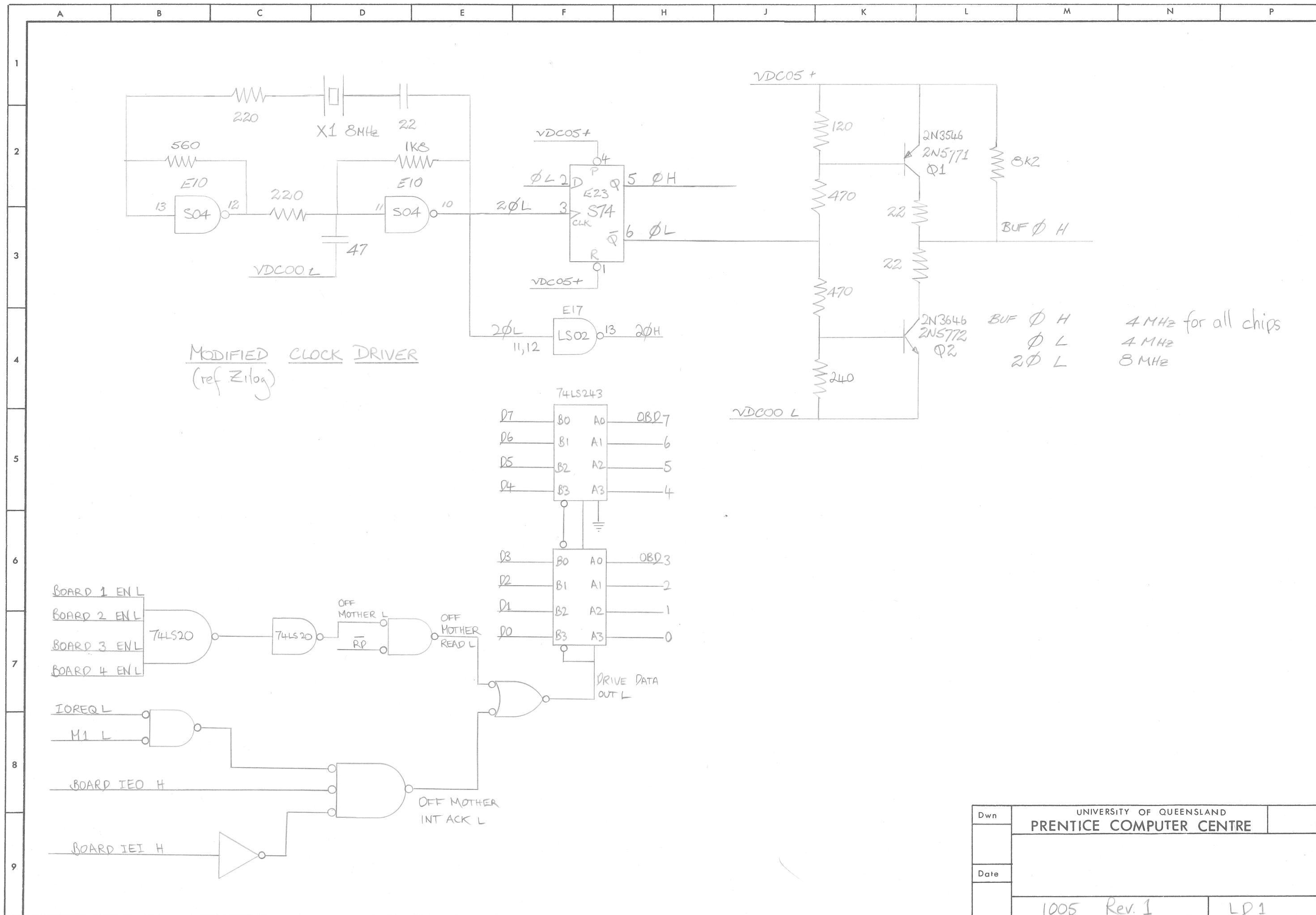
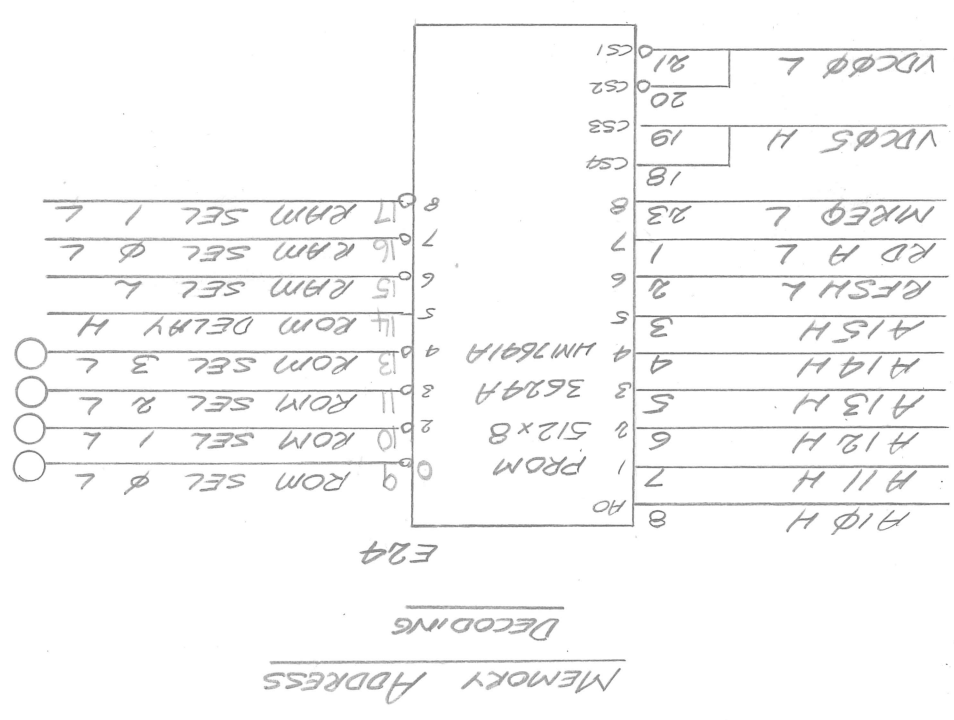
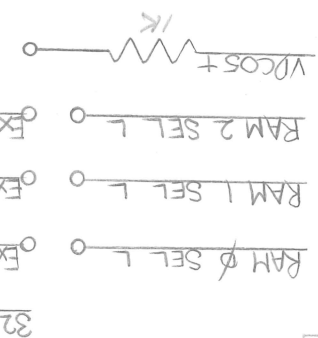


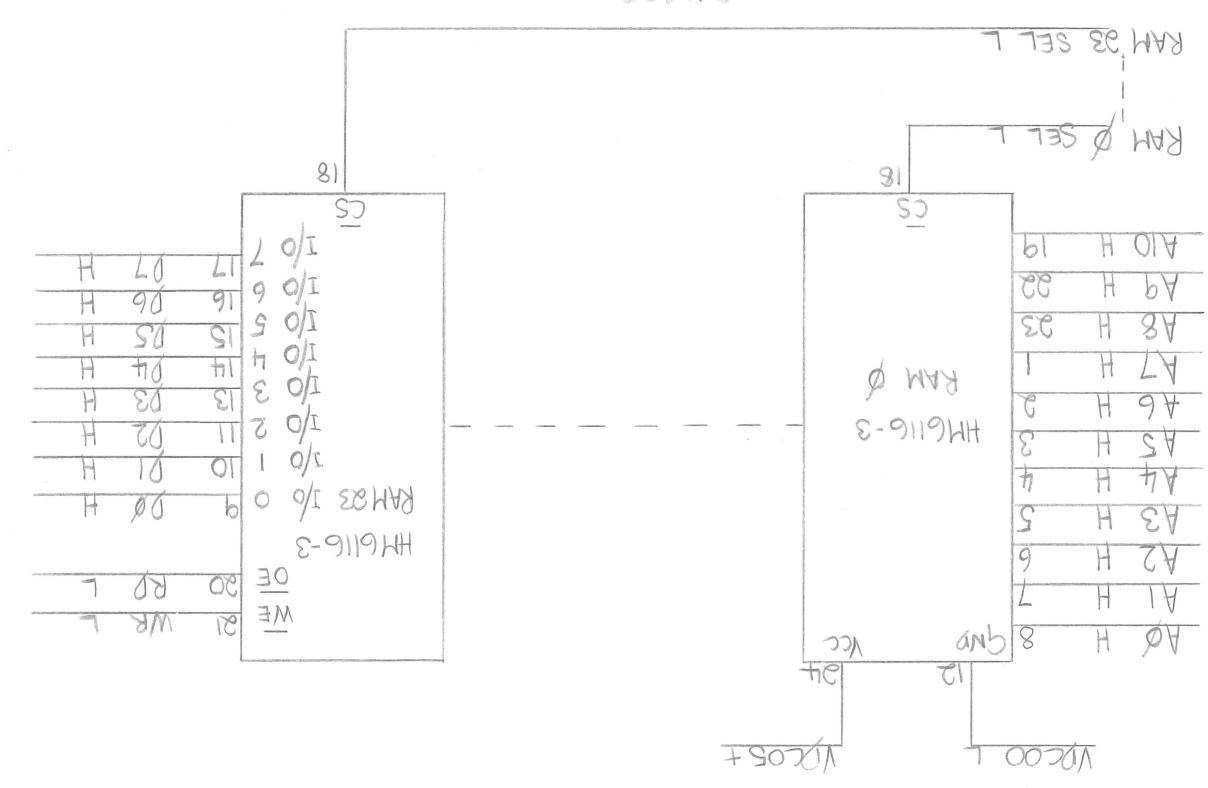
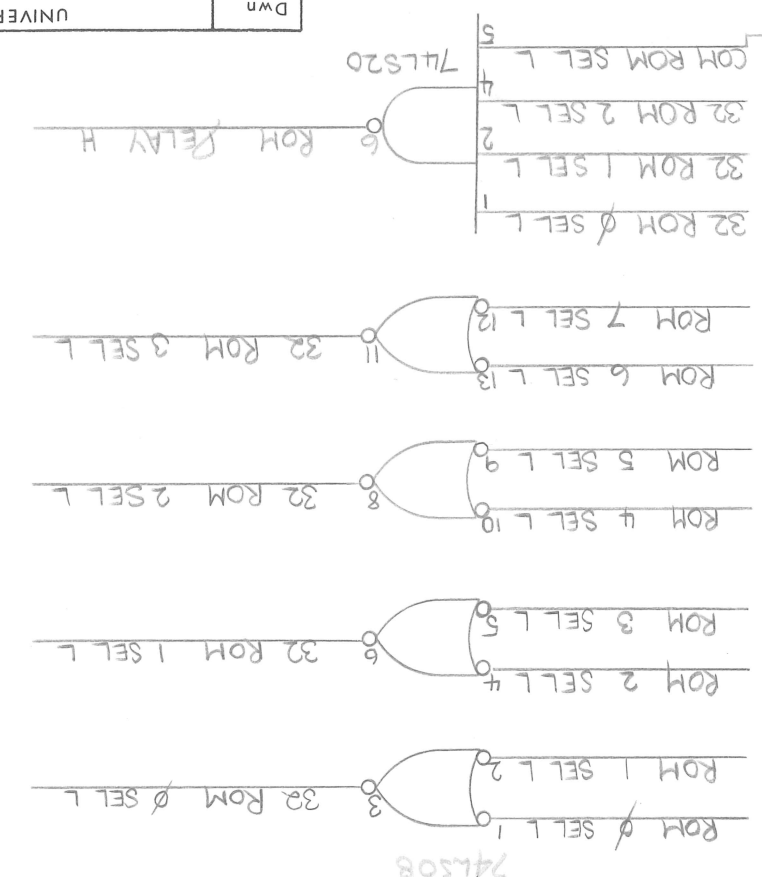
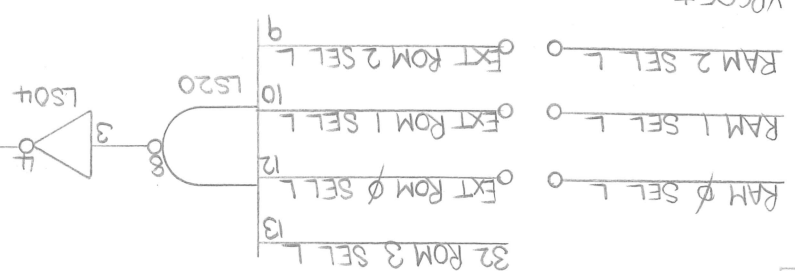
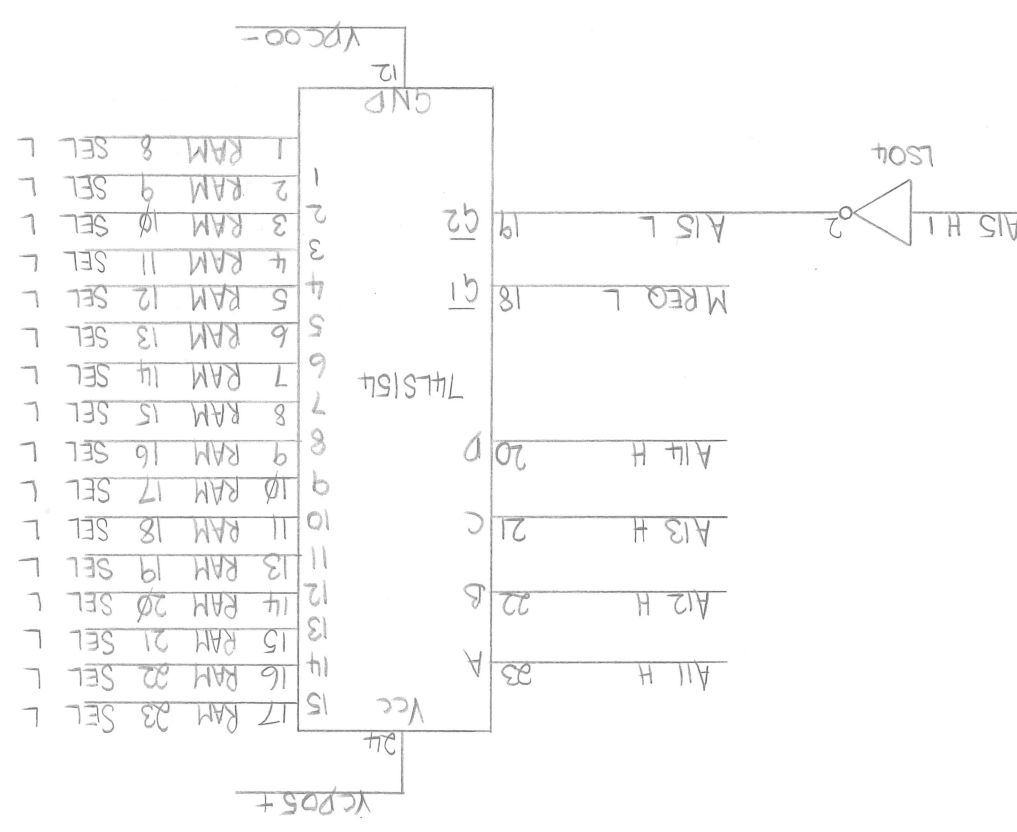




Notes: ROM may be substituted for RAM (0-2) by strapping RAM sel signals to EXT ROM. Use only 2716 ROMs. STRAP UNUSED EXT ROM INPUTS HIGH



1	RAM 0 SEL L
2	RAM 1 SEL L
3	RAM 2 SEL L
4	RAM 3 SEL L
5	RAM 4 SEL L
6	RAM 5 SEL L
7	RAM 6 SEL L
8	RAM 7 SEL L
9	RAM 0 SEL L
10	RAM 1 SEL L
11	RAM 2 SEL L
13	RAM 3 SEL L
14	RAM 4 SEL L
15	RAM 5 SEL L
16	RAM 6 SEL L
17	RAM 7 SEL L



LABRAK CHOS STATIC MEMORY SUBSYSTEM

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1.3.82
Date
MK.
Dwn

A	B	C	D	E	F	H	J	K	L	M	N	P
---	---	---	---	---	---	---	---	---	---	---	---	---

9

8

7

6

5

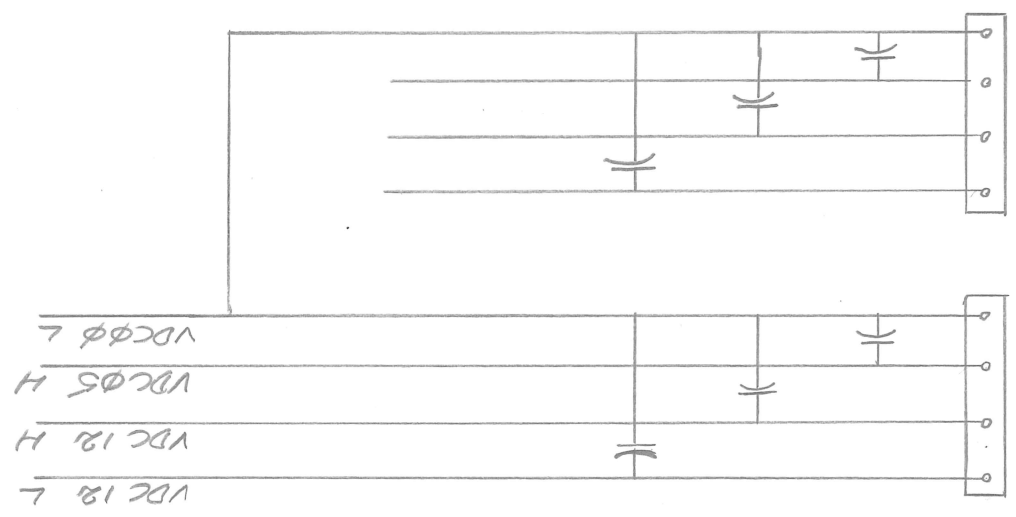
4

3

2

1

SPARE GATES:



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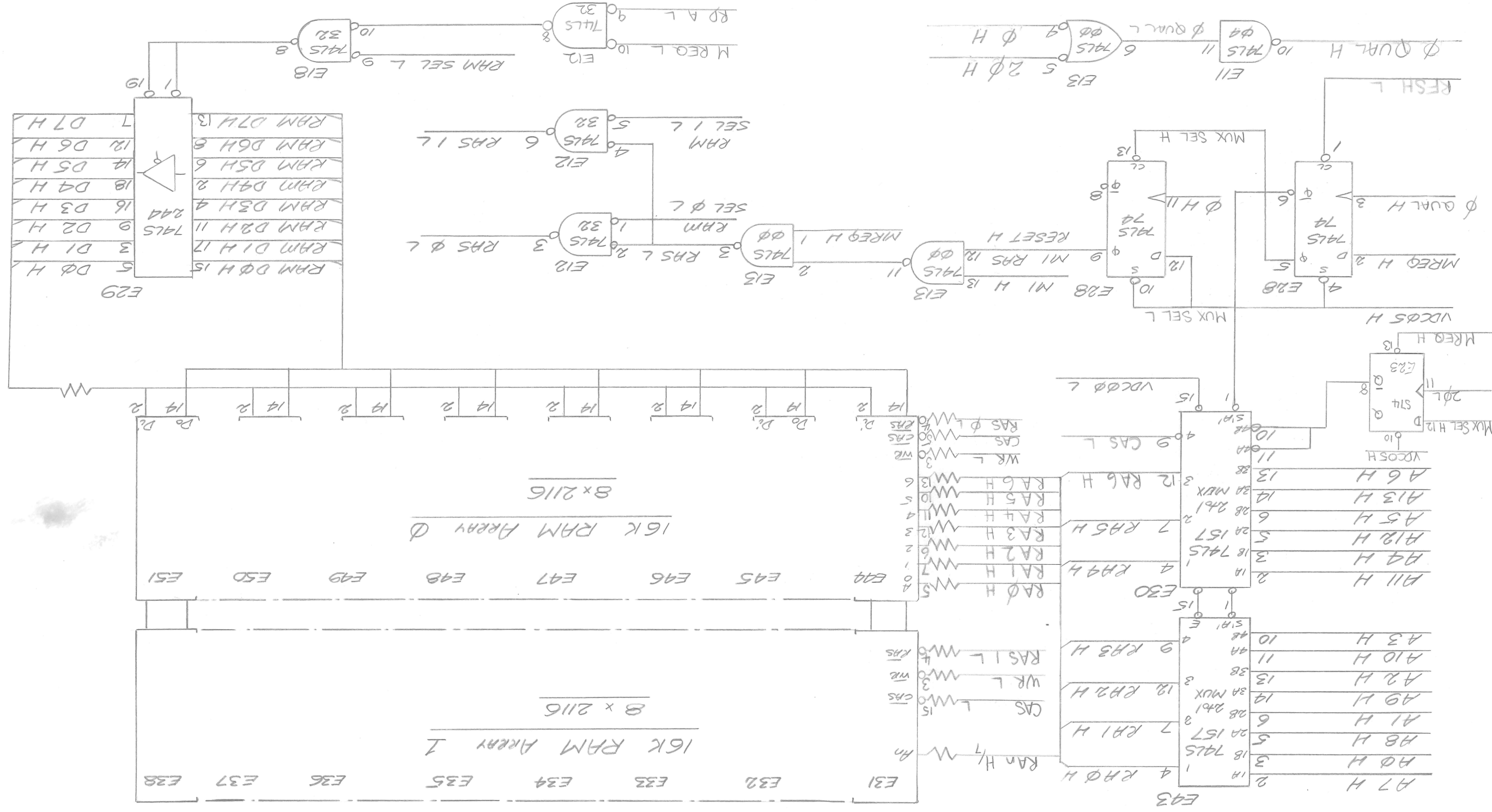
1005 Rev 1

LD 8

Date _____

DWN

1. PULLING RESISTORS IN ALL RAM LINES 3352



A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
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	A	B	C	D	E	F	H	J	K	L	M	N	P
9													
8													
7													
6													
5													
4													
3													
2													
1													

[illegible]

												9
												8
												7
												6
												5
												4
												3
												2
												1
A	B	C	D	E	F	H	J	K	L	W	N	P

		Date										
		Dwn										
		PRENTICE COMPUTER CENTRE UNIVERSITY OF QUEENSLAND										

Dwn	
Date	

												9
												8
												7
												6
												5
												4
												3
												2
												1
A	B	C	D	E	F	H	J	K	L	W	N	P

Date
Dwn

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