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FIELD MAINTENANCE PRINT SET

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D-CS-M8189-Ø-K10	BAUD RATE & -12V
D-CS-M8189-Ø-K11	CONFIGURATION GUIDE
B-DD-KEF11-BB	CIS MICROCODE HYBRID

UNIT VARIATIONS COVERED BY THIS PRINT SET
KDF11-BA
KDF11-BB
KDF11-BC
KDF11-BD
KDF11-BE

KDF11-B

Field Maintenance Print Set

Digital Equipment Corporation

Print Set Part Number MP- Ø1236

REV C

NUMBER KDF11-B-1

CODE TC

SIZE B

NR REVISION HISTORY

REV.	ECO NUMBER	DATE
A	INITALIZE	6/17/81
B	KDF11-B-ML0001	12APR82
C	KDF11-B-ML0002	4JUN83

DRN.	P. BROSNIHAN	DATE	4/4/81
CHK'D.	G. MARINI	DATE	4/4/81
DES. ENG.	Jay Nichols	DATE	22-JUN-81
RESP. ENG.	C. A. Valentine	DATE	22-JUN-81
FIELD SERVICE	G. Marini	DATE	23-JUN-81
NEXT HIGHER DOC.	11/23-B		

TITLE

digital

FIELD MAINTENANCE PRINT SET
KDF11-B

DOCUMENT NUMBER

SIZE	CODE	NUMBER	REV.
B	TC	KDF11-B-1	C

SHEET 1 OF 1

ML 3

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TABLE 1 BOOT/DIAG. SELECTION GUIDE FOR SWITCH PACK E102

SWITCH	ON	OFF
S1	EXECUTE CPU TEST	SKIP CPU TEST
S2	EXECUTE MEMORY TEST	SKIP MEMORY TEST
S3	EXECUTE DECNET BOOT PROGRAM SELECTED BY S4-S7 PER TABLE 2.	EXECUTE STANDARD BOOT PROGRAM PER SWITCH S4
S4	EXECUTE DIALOGUE BOOT PROGRAM. OPERATOR RESPONDS WITH MNEMONIC PER TABLE 3.	EXECUTE AUTOMATIC (TURNKEY) BOOT PROGRAM SELECTED BY S5-S8 PER TABLE 3.

TABLE 2 DECNET BOOT DEVICE SELECTION (S3 ON)

S4	S5	S6	S7	DEVICE
ON	X	X	X	DUV11
OFF	ON	X	OFF	DLV11-E
OFF	ON	X	ON	DLV11-F

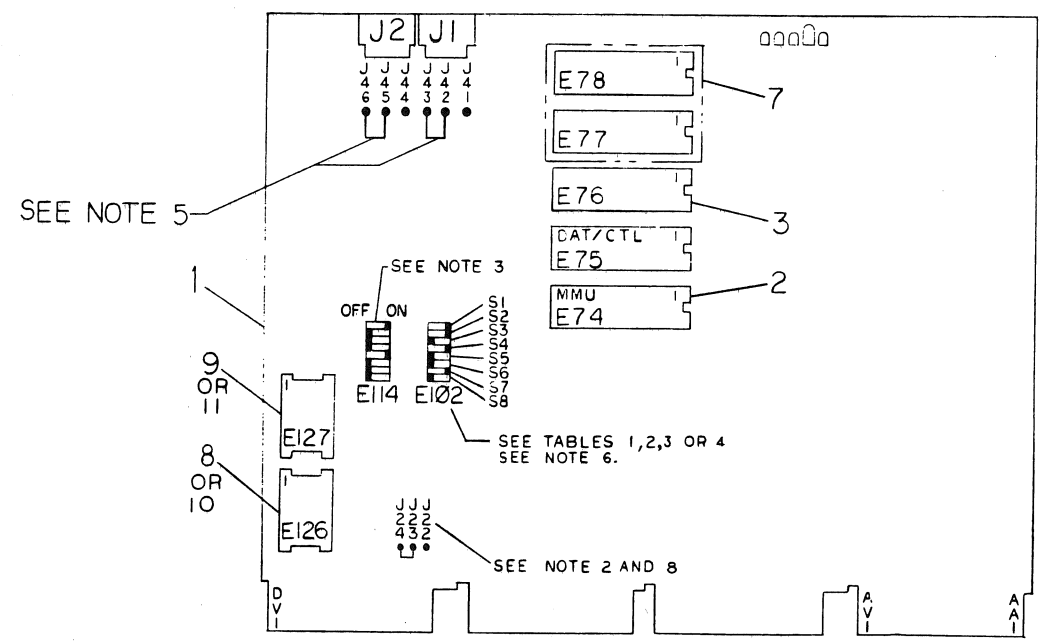
NOTE: X = DON'T CARE

TABLE 3 STANDARD BOOT DEVICE SELECTION (S3 OFF)

MNEMONIC	S5	S6	S7	S8	DEVICE
DKn; n<8	OFF	OFF	OFF	ON	RK05
DLn; n<4	OFF	OFF	ON	OFF	RL01/RL02
DDn; n<2	OFF	OFF	ON	ON	TU58
DXn; n<2	OFF	ON	OFF	OFF	RX01
DYn; n<2	OFF	ON	ON	OFF	RX02

LEGEND

NUMBER	DESCRIPTION
KDF11-BA	M8189-ØØ PLUS KTF11-AA & BOOT/DIAG. ROMS, P/N: 23-339E2-00 & 23-340E2-00
KDF11-BB	M8189-ØØ PLUS KTF11-AA, KEF11-AA & BOOT DIAG. ROMS P/N: 23-339E2-00 & 23-340E2-00
KDF11-BC	M8189-ØØ PLUS BOOT/DIAG. ROMS P/N: 23 339E2-00 & 23-340E2-00
KDF11-BD	M8189-00 PLUS KTF11 AA, KEF11-BB & BOOT/DIAG. ROMS P N: 23-339E2-00 & 23-340E2-00
KDF11-BE	M8189-00 PLUS KTF11-AA & 16KB BOOT/DIAGNOSTIC ROMS, P/N: 23-157E4 & 23-158E4. CONFIG. EXT. BAUD SEL.



NOTES:

1. WHEN INSTALLING ITEMS 2,3,8&9 MAKE SURE THAT PIN 1 IS LOCATED AS SHOWN.
2. FOR VARIATIONS-BA,BB,BC AND -BD WHEN ITEMS 8 & 9 ARE MASKED ROMS CONNECT J23 TO J24 WITH J22 NOT CONNECTED. WHEN ITEMS 8 & 9 ARE EPROMS CONNECT J22 TO J23 WITH J24 NOT CONNECTED.
3. BAUD RATE SELECTION. SEE D-CS-M8189-0-K11. SETTINGS SHOWN PRODUCE 9600 BAUD EACH LINE.
4. KEF11-BB=CIS MICROCODE HYBRID. CONTAINS CIS MICROCODE TO IMPLEMENT THE COMMERCIAL INSTRUCTION SET.
5. CONNECT J45 TO J46 WITH J44 NOT CONNECTED AND J43 TO J42 WITH J41 NOT CONNECTED FOR INTERNAL BAUD RATE GENERATOR ON-BA,-BB,-BC&BD VARIATIONS. CONNECT J45 TO J44 WITH J46 NOT CONNECTED AND J41 TO J42 WITH J43 NOT CONNECTED FOR EXTERNAL BAUD RATE GENERATOR ON -BE VARIATION.
6. USE TABLES 1,2 AND 3 FOR KDF11-BA,BB,BC,BD. USE TABLE 4 FOR KDF11-BE.
7. TO DIFFERENTIATE BETWEEN-BA AND-BE, STAMP MODULE HANDLE (SEE DETAIL "A" FOR PLACEMENT) WITH INDELIBLE INK AND CORRECT RUBBER STAMP; KDF11-BA OR KDF11-BE.
8. FOR VARIATION-BE, CONNECT J24 TO J23 WITH J22 NOT CONNECTED.

CAUTION: OFF SHEET PARTS LIST EXISTS, SEE K-PL-KDF11-B-DBP

REVISIONS

CHK	CHANGE NO.	REV.
	INITIAL	A
[illegible]	KDF11-B-ML001 [illegible] 12-APR-82 C. VALENTINE [illegible] (HFC) 5-13-82	B
	KDF11-B-ML002 S CORMIER 25MAY83 M. O'RIORDAN M. O'Riordan 1-Jun-83	C

DESCRIPTION	DWG./PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES ±0° 30'

SURFACE QUALITY IN MICROINCHES

CLASS OF ACCURACY (CHECK ONE)	OVER 0 TO 0.2	OVER 0.2 TO 1.2	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 80.0
MEDIUM	±.004	±.008	±.012	±.016	±.024	±.04
PREFERRED	±.012	±.016	±.025	±.04	±.063	±0.1

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL —

FINISH —

DRN. H. Cullison

CHK'D [illegible]

ENG. [illegible] 22-Jun-81

PROJ. ENG [illegible] 22-Jun-81

PROD. [illegible] 22 Jun-81

NEXT HIGHER ASSY. B-DD-KDF11-B

SCALE NONE

SHEET 1 OF 3

FIRST USED ON 11/23-B

digital

TITLE KDF11-B CPU UNIT ASSEMBLY

SIZE D CODE UA NUMBER KDF11-B-Ø REV. C

DIST.

DEC FORM NO. DRD 100-C

SWITCHES

1 = ON
0 = OFF
X = DOES NOT EFFECT CONDITION SELECTED

TABLE 4 BOOTSTRAP DIAGNOSTIC CONFIGURATION SWITCHES

SWITCH SETTING								FUNCTION
8	7	6	5	4	3	2	1	
X	X	0	0	0	0	0	0	INHIBIT POWER ON AUTO BOOT
0	X	X	X	X	X	X	X	CONSOLE TERMINAL IS NOT AN ANSI MODE SCOPE
1	X	X	X	X	X	X	X	CONSOLE TERMINAL IS AN ANSI MODE SCOPE
X	1	X	X	X	X	X	X	* EXECUTE QUICK VERIFY MEMORY DIAGNOSTICS
X	X	0	0	0	0	1	0	SELECT TU58 DEVICE 0
X	X	0	0	0	0	1	1	SELECT TU58 DEVICE 1
X	X	0	0	0	1	0	0	SELECT RX01 DEVICE 0
X	X	0	0	0	1	0	1	SELECT RX01 DEVICE 1
X	X	0	0	0	1	1	0	SELECT RX02 DEVICE 0
X	X	0	0	1	0	0	0	SELECT RX02 DEVICE 1
X	X	0	0	1	0	0	0	SELECT MSCP DEVICE 0
X	X	0	0	1	0	0	1	SELECT MSCP DEVICE 1
X	X	0	0	1	0	1	0	SELECT MSCP DEVICE 2
X	X	0	0	1	0	1	1	SELECT MSCP DEVICE 3
X	X	0	0	1	1	0	0	SELECT MSCP DEVICE 4
X	X	0	0	1	1	0	1	SELECT MSCP DEVICE 5
X	X	0	0	1	1	1	0	SELECT MSCP DEVICE 6
X	X	0	0	1	1	1	1	SELECT MSCP AUTO BOOT SEQUENCER (SNIFFER BOOT)
X	X	0	1	0	0	0	0	SELECT RL01/RL02 DEVICE 0
X	X	0	1	0	0	0	1	SELECT RL01/RL02 DEVICE 1
X	X	0	1	0	0	1	0	SELECT RL01/RL02 DEVICE 2
X	X	0	1	0	0	1	1	SELECT RL01/RL02 DEVICE 3
X	X	0	1	1	0	0	0	RESERVED FOR FUTURE DEVICES
X	X	1	1	0	1	1	1	
X	X	1	1	1	0	0	0	SELECT DECNET DUV11
X	X	1	1	1	0	0	1	SELECT DECNET DLV11-E
X	X	1	1	1	0	1	0	SELECT DECNET DLV11-F
X	0	1	1	1	1	1	1	LOOP SELF TEST BUT DO NOT EXECUTE MEMORY DIAGNOSTIC
X	1	1	1	1	1	1	1	LOOP SELF TEST AND MEMORY DIAGNOSTIC
1	1	0	0	1	1	1	1	

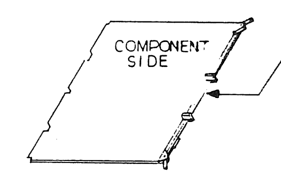
* THE FIRST 48 KB OF MEMORY WILL ALWAYS BE TESTED REGARDLESS OF SWITCH POSITION. THERE MUST BE A MINIMUM OF 16 KB OF MEMORY TO RUN WITH THESE ROMS.

SWITCH REGISTER FORMAT

- O BITS 6:4 ARE CONTROLLER TYPE ID, BITS 3:1 ARE UNIT NUMBER SELECT.
- O BITS 6:3 ARE CONTROLLER TYPE ID, BITS 2:1 ARE UNIT NUMBER SELECT.
- O BITS 6:2 ARE CONTROLLER TYPE ID, BITS 1 IS UNIT NUMBER SELECT.
- O BITS 6:4 = 1 IS DECNET IDENTIFIER, BITS 3:1 SELECT LINK TYPE.
- O BITS 6:4 IS DECNET IDENTIFIER, BITS 3:1 SELECT LINK TYPE.
- O BITS 6:1 = 1 IS LOOP SELFTEST AND CONDITIONALLY MEMORY DIAGNOSTIC.

ALL UNIMPLEMENTED SWITCH CONFIGURATIONS WILL CAUSE AN ERROR MESSAGE TO BE PRINTED AND CONTROL PASSED TO CONSOLE DIALOGUE ROUTINE.

DETAIL "A"



WITH COMPONENT SIDE UP STAMP MODULE HANDLE EDGE JUST RIGHT OF CENTER SO THAT STAMP IS VISIBLE WHEN MODULE IS INSERTED IN BACKPLANE.

REVISION HISTORY

REV	ECO NUMBER	DATE

TITLE KDF11-B CPU UNIT ASSEMBLY

SIZE	CODE	DOCUMENT NUMBER	REV
D	UA	KDF11-B-0	C

SCALE NONE SHEET 2 OF 3

DRD 137C EN-01204-18-REVA(305)

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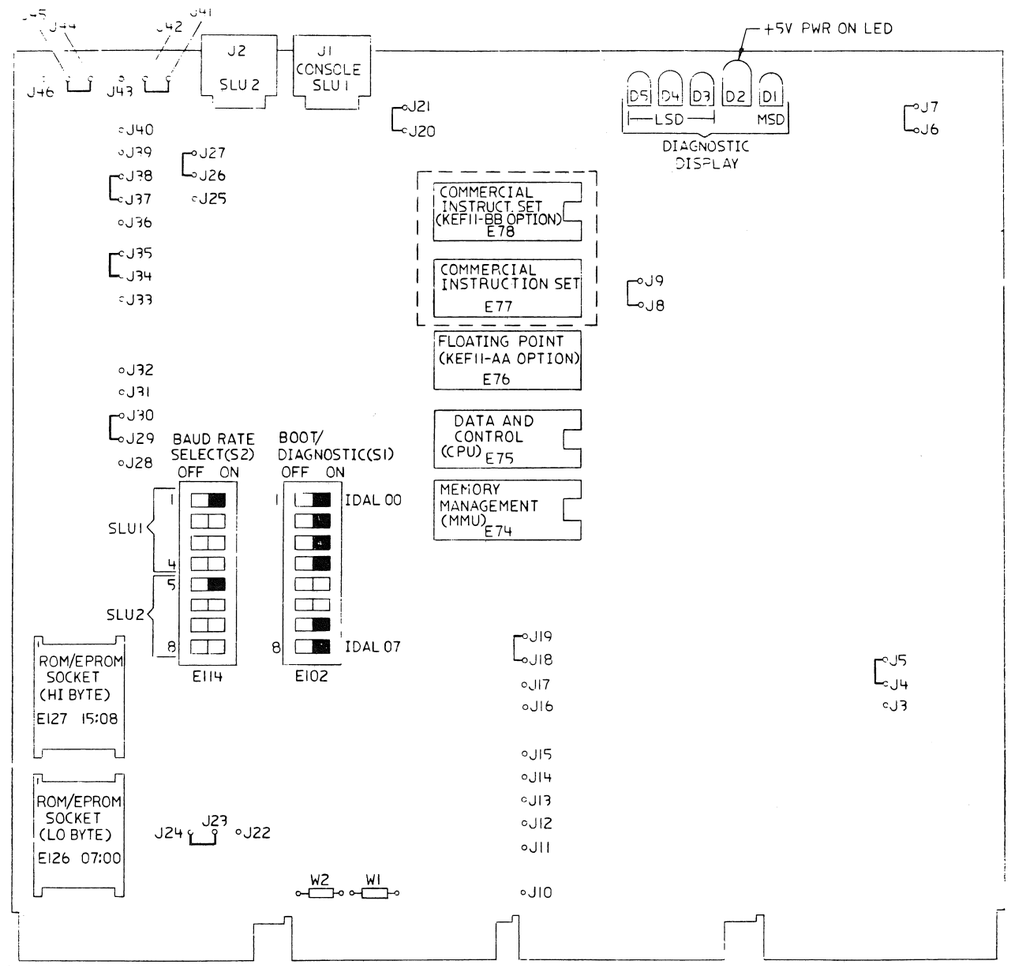

KDF11-BE JUMPER, SWITCH & DIAGNOSTIC DISPLAY LOCATIONS

NOTES

1. INSTALLED JUMPERS SHOW THE FACTORY CONFIGURATION.
2. SWITCHES S1-1,2,3,4,7,8 & S2-1,5 ARE SHOWN IN "ON" POSITION.

REVISION HISTORY		
REV	ECO NUMBER	DATE

TITLE KDF11-B CPU UNIT ASSEMBLY

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV
D	UA	KDF11-B-0	C
SCALE NONE		SHEET 3 OF 3	

DRD 137C

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QUANTITY PER VARIATION BA	BB	BC	BD	BE
1	1	D-UA-M8189-0-0	M8189-00	KDF11-B QD CPU,Q OR Q22-BUS PDP1	1	1	1	1	1
2	2		2115542-01	DC 304 F11 MMU,FLOAT PT REG	1	1	-	1	1
3	3	C-UA-5700001-0-0	5700001-00	HYBRID ASSY FLOATING POINT	-	1	-	-	-
4	4		23244E2-00	*** THIS ITEM IS NOT USED ***	-	-	-	-	-
5	5		23245E2-00	*** THIS ITEM IS NOT USED ***	-	-	-	-	-
6	6	C-UA-H3270-0-0	H3270-00	DLV11-J LOOPBACK TEST PLUG	1	1	1	1	1
7	7	K-PL-KEF11-BB-DBP	KEF11-BB	HYBRID CIS MICROCODE CHIP (HYBRI	-	-	-	1	-
8	8		23339E2-00	E2-04	1	1	1	1	-
9	9		23340E2-00	E2-04,	1	1	1	1	-
10	10		23157E4-00	E4-01,E4-05 ROM	-	-	-	-	1
11	11		23158E4-00	E4-01,E4-05 ROM	-	-	-	-	1

12 NOTE: ITEM #6, THE WRAP-AROUND-TEST JUMPER FOR CONNECTOR J2, IS NOT SHOWN ON UA DWG.
13 NOTE: FOR BULK INTERPLANT SHIPMENT OF MODULES REFER TO PACKAGING INSTRUCTION A-SP-3700053-0-0
14 NOTE: FOR SHIPMENT OF INDIVIDUAL MODULES REFER TO PACKAGING INSTRUCTION A-SP-3700069-0-0
15 NOTE: SEE DETAIL "A" AND NOTE 7 (SHEET 2 OF 2) FOR MODULE IDENTIFICATION STAMP.

REVISION HISTORY			BASIC PART NO: KDF11									
ENG	ECO NUMBER	REV	SECTION A OF A	DRN: P. BROSNIHAN	DATE: 21-JAN-81		D	I	G	I	T	A	L
	INITIAL	A	SECTION. VARIATION INDEX	CHK'D: G. MARINI	DATE: 27-MAY-81	TITLE PARTS LIST						
CV	KDF11-B-ML001	B	[A] BA,BB,BC,BD,BE			KDF11-B CPU UNIT ASSEMBLY						
MD	KDF11-B-ML002	C	[B]	DES.ENG.: C. VALENTINE	DATE: 21-JAN-81							
			[C]	RESP.ENG.: C. VALENTINE	DATE: 21-JAN-81	DOCUMENT NUMBER						
			[D]			SIZE	CODE	NUMBER		REV		
			[E]	MFG.ENG.: T. OLMO	DATE: 27-APR-81	K	PL	KDF11-B-DBP		C		
			[F]	ASSEMBLY NUMBER: C-UA-KDF11-B-0	TOP DOCUMENT NUMBER: #8-DD-KDF11-B			FILE NAME: Z2423C.PLS		EDIT # 2		

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SIZE	CODE	NUMBER	REV.
B	DD	M8189-Ø	D

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS			
		M8189-ØØ	KDF11-B CPU MODULE				
D-UA-M8189-Ø-Ø	2		KDF11-B CPU MODULE	A	A	A	B
K-PL-M8189-Ø-DBP	3		KDF11-B CPU MODULE	A	A	B	B
K-PC-M8189-Ø-DBC			P.C. DESIGN DATA BASE	C	C	C	C
		5Ø14313-ØØ	P.C. BOARD	C	C	C	C
D-MD-5Ø14313-Ø-Ø	6		DRILL & ETCH DRAWING	A	B	B	B
D-EC-5Ø14313-Ø-Ø	2		ETCH CUT DRAWING	A	A	A	A
K-CS-M8189-0-DBS			CIRCUIT DATA BASE	A	A	A	B
D-CS-M8189-Ø-K1	1		TIMING LOGIC & MIB DECODE	A	A	A	A
D-CS-M8189-Ø-K2	1		BUS CONTROL LOGIC	A	A	A	A
D-CS-M8189-Ø-K3	1		SERVICE, RESET & ODT LOGIC	A	A	A	A
D-CS-M8189-Ø-K4	1		F11 CHIPS & FIXED DATA	A	A	A	A
D-CS-M8189-Ø-K5	1		CDAL/BDAL INTERFACE	A	A	A	A
D-CS-M8189-Ø-K6	1		CDAL/IDAL INTERFACE	A	A	A	A
D-CS-M8189-Ø-K7	1		IDAL ADRS DECODE	A	A	A	A
D-CS-M8189-Ø-K8	1		BOOT & CLOCK LOGIC	A	A	A	B
D-CS-M8189-Ø-K9	1		CONSOLE & SECOND SLU	A	A	A	A
D-CS-M8189-Ø-K10	1		BAUD RATE & -12V	A	A	A	A
D-CS-M8189-Ø-K11	1		CONFIGURATION GUIDE	A	A	A	B

NOTES:

REVISIONS			
REV.	B	C	D
CHG NO.	ML001	ML002	ML003
DATE	9 83	23JAN83	26SEP83

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DRB 126

digital

USED ON OPTION/MODEL
KDF11-B

DRN.	R. BARILONE	2DEC80
CHK'D	D. DROZD	22JAN81
ENG.	J. NICHOLS	13APR81
PROD.	T. OLMO	13APR81

TITLE: KDF11-B CPU MODULE

SIZE	CODE	NUMBER	REV
B	DD	M8189-Ø	D

SHEET 1 OF 1

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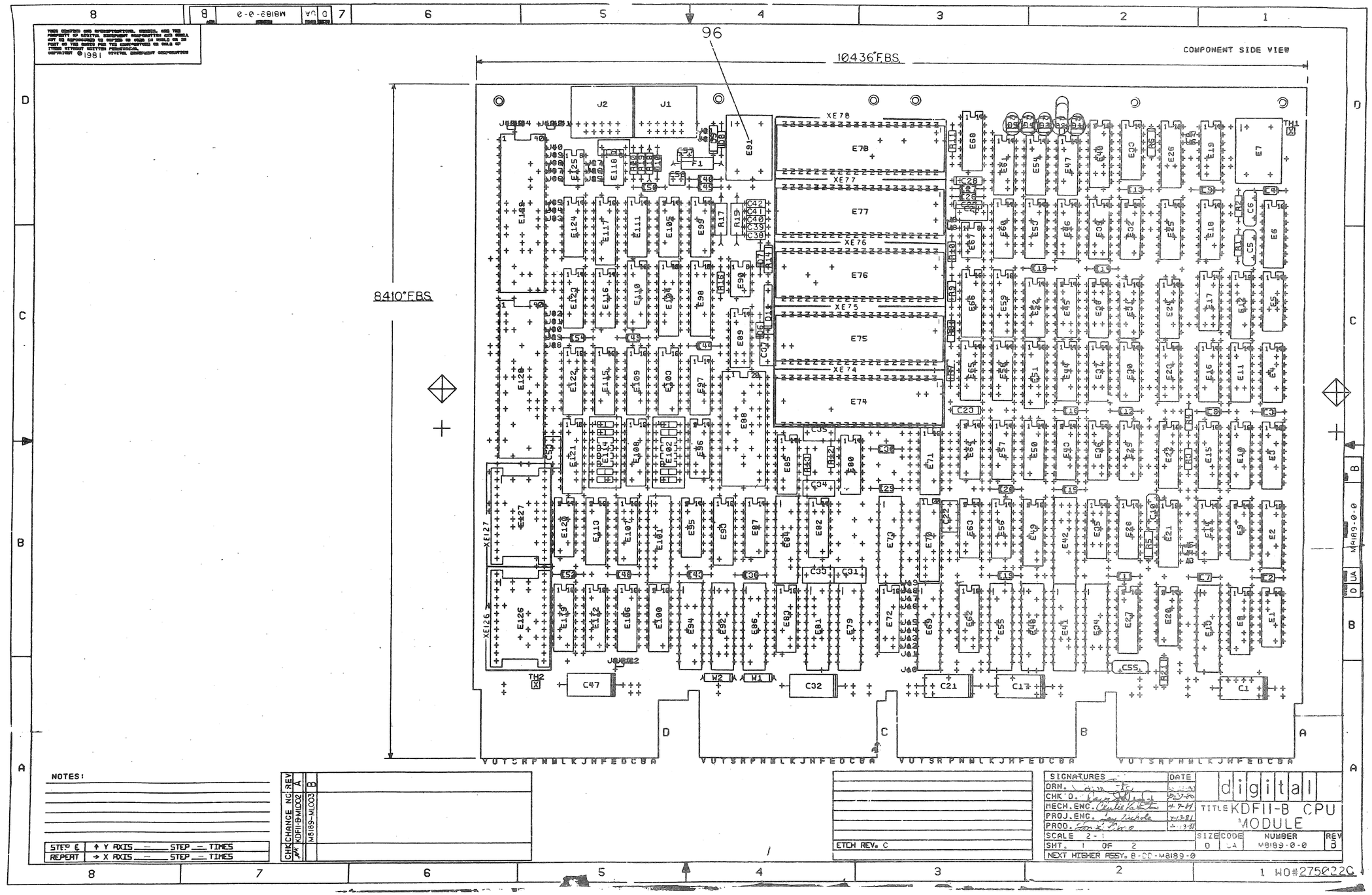

NOTES:

STEP & REPEAT	
↑ Y AXIS ___ STEP ___ TIMES	
→ X AXIS ___ STEP ___ TIMES	

CHK CHANGE NO.	REV
KDFII-B-MLOO2	A
M8189-MLOO3	B

ETCH REV. C

SIGNATURES	DATE
DRN.	
CHK'D.	8-27-80
MECH. ENG.	4-7-81
PROJ. ENG.	4-13-81
PROD.	4-13-81

digital

TITLE KDFII-B CPU MODULE

SCALE 2 - 1 | SIZE D | CODE CA | NUMBER M8189-0-0 | REV B

SHT. 1 OF 2

NEXT HIGHER ASSY. B-CC-M8189-0

1 WO#275022C

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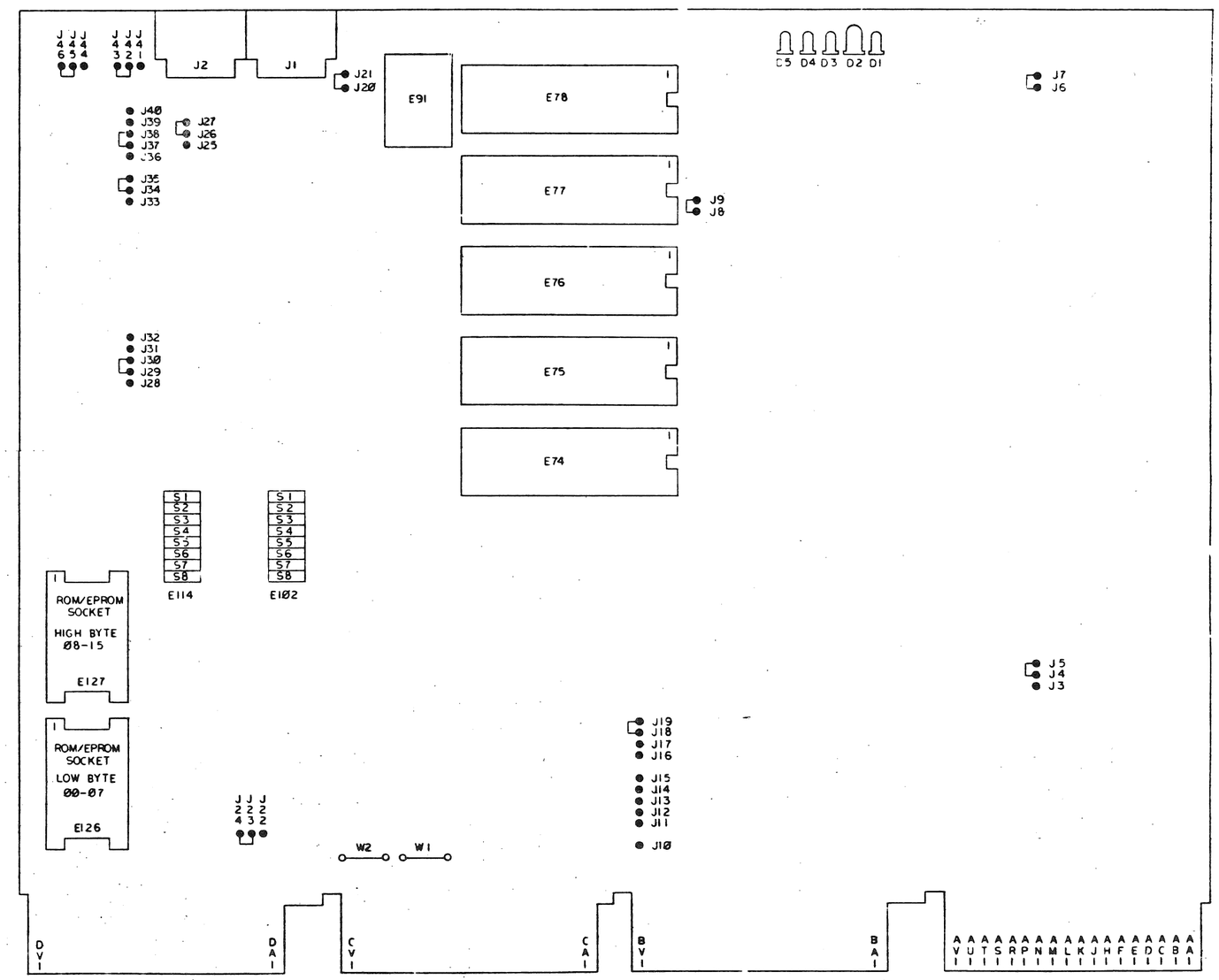
JUMPER TABLE			
ITEM NO	DESCRIPTION	FROM	TO
97	MINI JUMPER	J4	J5
		J6	J7
		J8	J9
		J18	J19
		J20	J21
		J23	J24
		J26	J27
		J29	J30
		J34	J35
		J37	J38
		J42	J43
		J45	J46

SEE NOTE 1

NOTES:

1. CONNECT J24 TO J23 WITH J22 NOT CONNECTED TO ENABLE K8 BTRA 13 H TO PIN 21 OF SOCKETS E126 AND E127. CONNECT J22 TO J23 WITH J24 NOT CONNECTED TO ENABLE +5V TO PIN 21 OF SOCKETS E126 AND E127.



REVISION HISTORY		
DATE	ECO NUMBER	REV.

TITLE KDF11-B CPU MODULE

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV.
D	UA	M8189-0-0	B
SCALE		SHEET 2 OF 2	

AUTOMATED BY PRTLST.3P(44)

P A R T S L I S T

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
1	1	D-MD-5014313-0-0	5014313-00	DRILL AND ETCH FOR M8189	1	
2	2		1000022-00	270.0 MMF 100V 5%200PPM MICA	1	C10
3	3		1000024-00	470.0 MMF 100V 5%200PPM MICA	3	C5,C6,C55
4	4		1001610-00	.01 MFD 50V +80-20% Z5U CER	3	C26,C27,C30
5	5		1012784-00	.047 MFD 50V +80-20% CER	29	C2-C4,C7-C9,C11-C16,C18-C20,C23,
						CONT C25,C28,C29,C36,C43-C46,C48-C50,
						CONT C52,C54
6	6		1016681-00	.47 MFD 50V +80-20% CER	14	C22,C24,C31,C33-C35,C37-C42,C51,
						CONT C53
7	7		1017472-00	10 MFD 35V +50-10% AL EL	5	C1,C17,C21,C32,C47
8	8		1011740-02	1800.0 MMF 50V 10% CER	2	C56,C57
9	9		1109977-00	1N 749A VZ= 4.3 5%	1	D9
10	10		1112689-00	LED .8MCD@16MA VF=5V	4	D1,D3-D5
11	11		1114384-00	LED 105MW 35MA GREEN	1	D2
12	12		1100114-00	D 664 QS\75PCB PIV= 25V SP	3	D6-D8
13	13		1110967-00	1N 4005 PIV=600 I= 1A D041 SI	1	D10
14	14		1105508-00	1N 823 VZ= 6.2 5% .40W Y	1	D11
15	15		1213506-04	PCB HEADER 09PIN(2X05).100CC 90D	2	J1,J2
16	16		1215006-06	SKT,IC 24PIN DIP TIN SOLD	2	XE126,XE127
17	17		1216116-00	SKT,IC 40PIN DIP GOLD CARR	5	XE74-XE78
18	18		1210929-02	FUSE, SUB-MINI 1.000A, 125V, A	1	F1
19	19		1211164-04	SW,DIP 08POS/1PST 5VDC100MA F	2	E102,E114
20	20		1213113-01	HANDLE,MODULE,	1	
21	21		1300229-00	100.0 .25 W 5.0 % CF	1	R7
22	22		1300316-00	470.0 .25 W 5.0 % CF	3	R6,R12,R16
23	23		1300365-00	1.0 K .25 W 5.0 % CF	4	R3,R4,R8,R11
24	24		1300488-00	12.0 K .25 W 5.0 % CF	2	R19,R20
25	25		1301322-00	180.0 .25 W 5.0 % CF	1	R13
26	26		1301808-00	22.0 K .25 W 5.0 % CF	1	R18
27	27		1302177-00	47.0 K .25 W 5.0 % CF	2	R1,R2

REVISION HISTORY			BASIC PART NO: M8189										
ENG	ECO NUMBER	REV	SECTION A OF A	DRN: R. BUREAU	DATE: 11-JUL-80		D	I	G	I	T	A	L
---	INITIAL	A	SECTION.VARIATION INDEX	CHK'D: BOB BARILONE	DATE: 11-JUL-80	TITLE PARTS LIST							
SC	M8189-ML002	B	[A] 00			KDF11-B CPU MODULE							
			[B]	DES.ENG: C.A. VALENTINE	DATE: 14-APR-81								
			[C]										
			[D]										
			[E]	RESP.ENG.: JAY NICHOLS	DATE: 14-APR-81	DOCUMENT NUMBER							
			[F]										
			[H]			SIZE	CODE	NUMBER				REV	
			[J]	MFG.ENG.: TOMAS OLMO	DATE: 14-APR-81	K	PL	M8189-0-DBP				B	
			[K]										
			[L]										
			[M]	ASSEMBLY NUMBER: D-UA-M8189-0-0	TOP DOCUMENT NUMBER: B-DD-M8189-0-0	FILE NAME: Z1037B.PLS						EDIT # 18	
			[N]										

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AUTOMATED BY PRTLST.3P(44)

P A R T S L I S T

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
28	28		1302602-00	56.0 .25 W 5.0 % CF	1	R5
29	29		1309422-00	5.10 .25 W 5.0 % CF	2	R9,R10
30	30		1311003-01	R NETWORK 14-180 14-390 16PIN	3	E8,E27,E62
31	31		1301320-00	1.20 K .25 W 5.0 % CF	1	R21
32	32		1300005-03	R NETWORK 13-10K 5.0 % 14PIN	1	E123
33	33		1300005-07	R NETWORK 15-4.7K 5.0 % 16PIN	3	E72,E108,E122
34	34		1300228-00	100.0 .50 W 5.0 % CF	2	R15,R17
35	35		1303178-00	620.0 .25 W 5.0 % CF	1	R14
36	36		1811660-02	OSCILLATOR, XTAL 5.0688 MHZ	1	E91
37	37		1811660-20	OSCILLATOR, XTAL 26.666 MHZ	1	E7
38	38		1910544-00	74S74 FF-D DUAL,EDGE TRIGG	8	E17,E19,E29,E30,E36,E38,E43,E50
39	39		1910548-00	74S157 MUX 1 OF 2 (QUAD)	1	E15
40	40		1910550-00	74S174 FF-D HEX	5	E3,E10,E21,E26,E51
41	41		1910957-00	74S175 FF-D QUAD COMMON CLO	4	E12,E22,E40,E59
42	42		1911117-00	*** THIS ITEM IS NOT USED ***	-	
43	43		1911469-00	DEC 8640 RECEIVER,BUS,QUAD,U	3	E1,E20,E63
44	44		1909705-00	DEC 8881 NAND GATE-QUAD 2IN O	1	E9
45	45		1911675-00	74S138 DECODER/DEMUX 3-8 LI	1	E66
46	46		1911712-00	74S51 AND-OR GATE-INVERT D	1	E45
47	47		1912098-00	0026 DRIVER,MOS CLOCK,2	1	E90
48	48		1912388-00	74S02 NOR GATE-QUAD 2IN,PO	3	E37,E52,E56
49	49		1912389-00	74S08 AND GATE-QUAD 2IN,PO	4	E11,E28,E39,E96
50	50		1912647-00	LS257 MUX 1 OF 2 (QUAD)	6	E83,E100,E106,E110,E113,E119
51	51		1912649-00	LS75 LATCH 4BIT,BISTABLE	1	E49
52	52		1912697-00	LS174 FF-D HEX W/CLEAR	3	E93,E107,E112
53	53		1912730-00	DC 003 INTERRUPT,2 CIRCUIT	2	E98,E104
54	54		1912746-00	DEC 74S37 NAND GATE-QUAD 2IN	1	E61
55	55		1912801-00	LS02 NOR-GATE-QUAD 2IN	1	E85
56	56		1912803-00	LS04 INVERTER GATE,HEX	1	E89
57	57		1912804-00	LS05 INVERTER GATE-HEX 1I	2	E82,E87
58	58		1912805-00	LS08 AND GATE-QUAD 2IN,PO	1	E65
59	59		1912807-00	LS10 NAND GATE-TRIPLE 3IN	2	E25,E95
60	60		1912808-00	LS11 AND GATE-TRIPLE 3IN	1	E14
61	61		1912810-00	LS20 NAND GATE-DUAL 4IN	2	E53,E60
62	62		1912816-00	LS32 OR GATE-QUAD 2IN,POS	2	E120,E124
63	63		1912824-00	LS74 FF-D DUAL,EDGE TRIGG	4	E5,E80,E111,E64
64	64		1912846-00	LS155 DECODER,2 OF 4(DUAL)	3	E103,E109,E115
65	65		1912853-00	LS175 FF-D QUAD	1	E117
66	66		1912857-00	LS197 COUNTER,BINARY,PRESET	1	E105
67	67		1912858-00	LS221 ONE SHOT-DUAL,SCHMIT	1	E6
68	68		1912863-00	LS273 FF-D OCTAL W/CLEAR	1	E86
69	69		1912868-00	LS299 SHIFT REG. 8-BIT UNI	2	E92,E101
70	70		1913340-00	74S32 OR GATE-QUAD 2IN	4	E4,E44,E97,E116
71	71		1913462-00	74S240 OCTAL BUFFER,INVERTI	3	E42,E73,E79
72	72		1913671-00	74S374 FF-D OCTAL TRISTATE	1	E70
73	73		1913777-00	LS240 DRIVER,LINE,OCTAL,T	1	E94
74	74		1914085-00	74S260 NOR GATE-DUAL,POS	1	E23
75	75		1915218-00	LS245 TRANSCEIVER,BUS,OCT	2	E81,E84

D	I	G	I	T	A	L	TITLE	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
							KDF11-B CPU MODULE		K	PL	M8189-0-DBP	B

AUTOMATED BY PRTLST.3P(44)

P A R T S L I S T

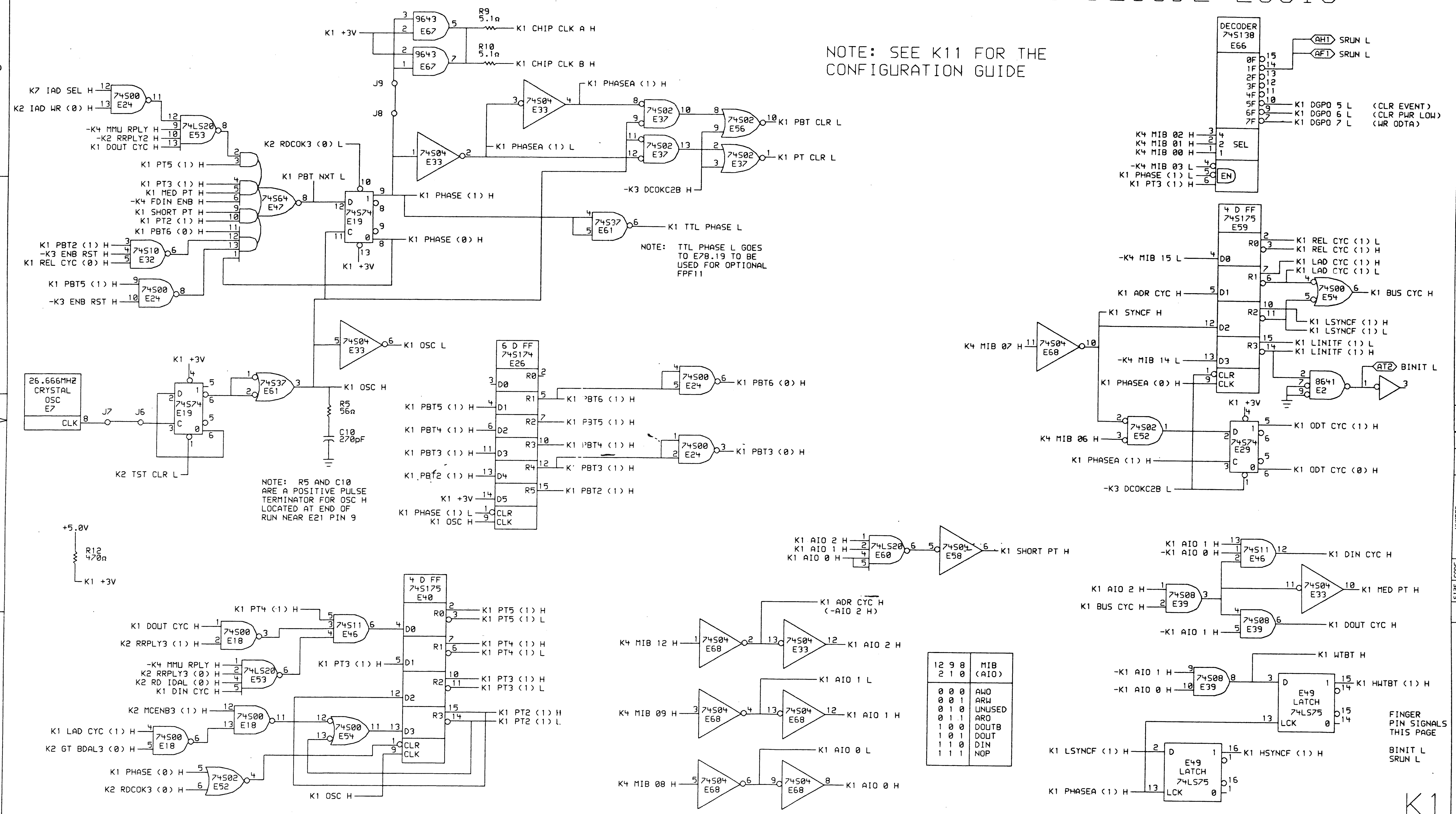
LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
76	76		1915305-00	AM 2908 TRANSCEIVER,BUS,LATCH	6	E13,E34,E41,E48,E55,E69
77	77		1915415-00	9636 DRIVER,DUAL,EIA RS-	1	E118
78	78		1915416-00	9637 RECEIVER,DUAL,RS-42	1	E125
79	79		1916028-01	9643 DRIVER,TTL TO MOS,D	1	E67
80	80		1910532-00	74S00 NAND GATE-QUAD 2IN	6	E16,E18,E24,E31,E35,E54
81	81		1910534-00	74S04 INVERTER GATE-HEX 1I	4	E33,E58,E68,E99
82	82		1910535-00	74S05 INVERTER GATE-HEX 1	1	E57
83	83		1910536-00	74S10 NAND GATE-TRIPLE 3IN	1	E32
84	84		1910537-00	74S11 AND GATE-TRIPLE 3INP	1	E46
85	85		1910542-00	74S64 A-O-I GATE 4-2-3-2	1	E47
86	87		2112623-00	DUAL BAUD RATE GEN/PROG DIVIDER,	1	E121
87	88		2113937-01	6402-1 UART,UNIV.,ASYNCHRO	2	E128,E129
88	91		23061C6-00	C6-01	1	E88
89	92		5700000-01	DAT/CTL HYBRID ASSY W/FP,DCF11-A	1	E75
90	93		9009149-00	PIN,STAKNG 0.0250DX0.345LG SQUAR	44	J3-J46
91	94		9009185-00	JUMPER, WIRE, INSULATED, BLACK B	2	W1,W2
92	95		9000024-01	EYELET,ROLLED 0.1210DX0.192	6	
93	96		9010213-01	SPACER,DUAL IN-LINE NYLN .450	1	
94	97		1218783-00	JUMPER 02POS(1X02).100CC	12	
95	98		1911579-00	8641 TRANSCEIVER,BUS,QUA	1	E2

D	I	G	I	T	A	L	TITLE	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
							KDF11-B CPU MODULE		K	PL	M8189-0-DBP	B

BASE TIMING - MCLK CTL

MIB DECODE LOGIC

NOTE: SEE K11 FOR THE CONFIGURATION GUIDE



12 9 8 2 1 0	MIB (AIO)
0 0 0	AWO
0 0 1	ARW
0 1 0	UNUSED
0 1 1	ARO
1 0 0	DOUTB
1 0 1	DOUT
1 1 0	DIN
1 1 1	NOP

K1

DRAWING 1 OF 11

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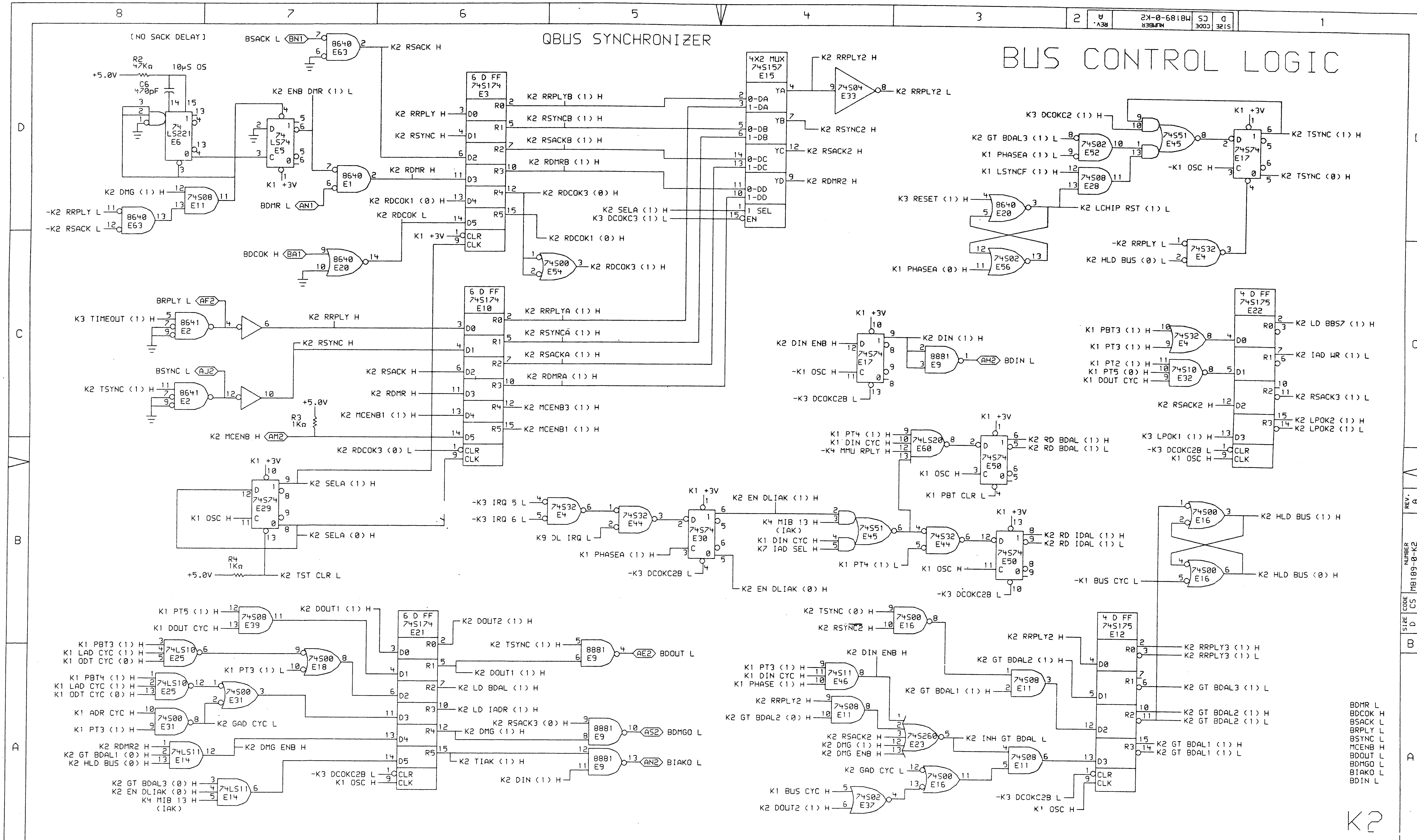
CHK	REVISIONS CHANGE NO.	REV

digital | DRN. | DATE 05-MAR-81 | ENG. | DATE 4-7-81
CHK. | DATE 4-13-81 | BOARD LOCATION: | SHEET 1 OF 1
[365,3132]M81891.DRW 04-MAR-81 16:55 | NEXT HIGHER ASSEMBLY: B-DD-M8189-0
FIRST USED ON OPTION/MODEL: KDF11-B
TITLE: TIMING LOGIC & MIB DECODE
SIZE D | CODE CS | NUMBER M8189-0-K1 | REV. A

BUS CONTROL LOGIC



DRAWING 2 OF 11

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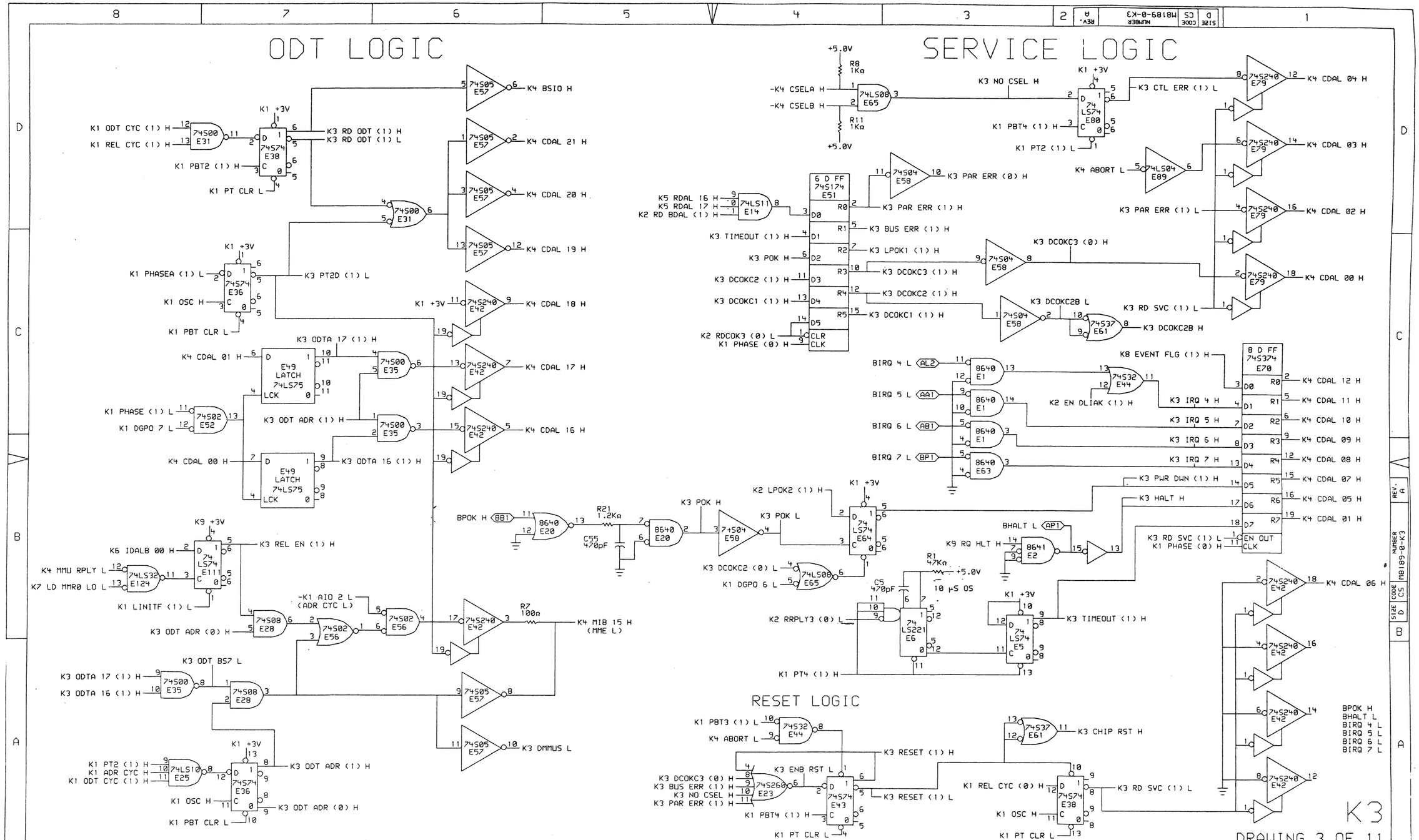
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. DATE 05-MAR-81 ENG. DATE
CHK. DATE 4-13-81 BOARD LOCATION:
SHEET 1 OF 1
L365.3132 M81892.DRW 04-MAR-81 17:09 NEXT HIGHER ASSEMBLY: B-DD-M8189-0
FIRST USED ON OPTION/MODEL: KDF11-B

TITLE: BUS CONTROL LOGIC

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K2	A



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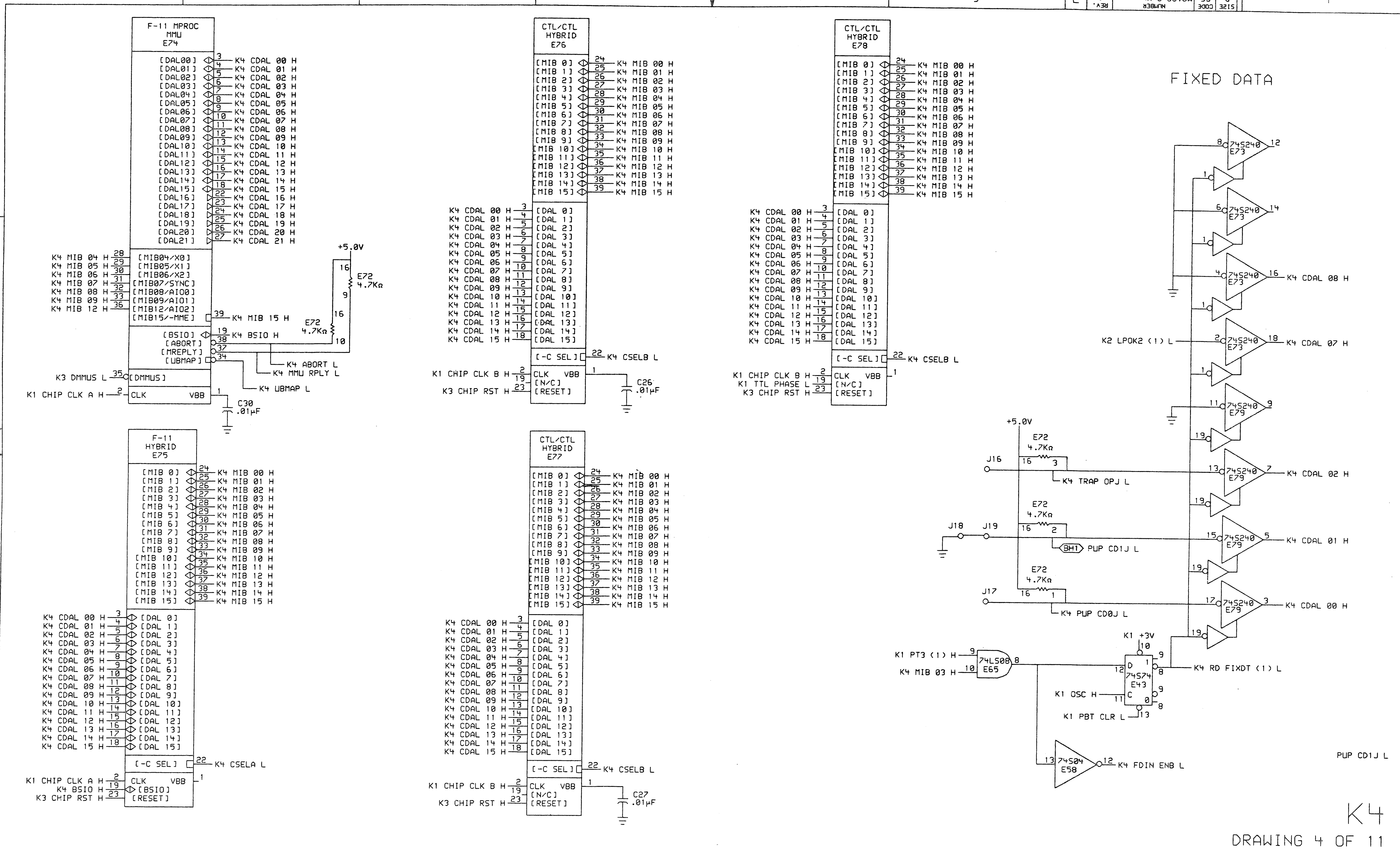
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. | DATE 05-MAR-81 | ENG. | DATE
CHK | DATE | BOARD LOCATION: | SHEET 1 OF 1
[365,3132]M81893.DRW | 04-MAR-81 17:15 | NEXT HIGHER ASSEMBLY: B-DD-M8189-0
FIRST USED ON OPTION/MODEL: KDF11-B

TITLE: SERVICE, RESET & ODT LOGIC

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K3	A



K4

DRAWING 4 OF 11

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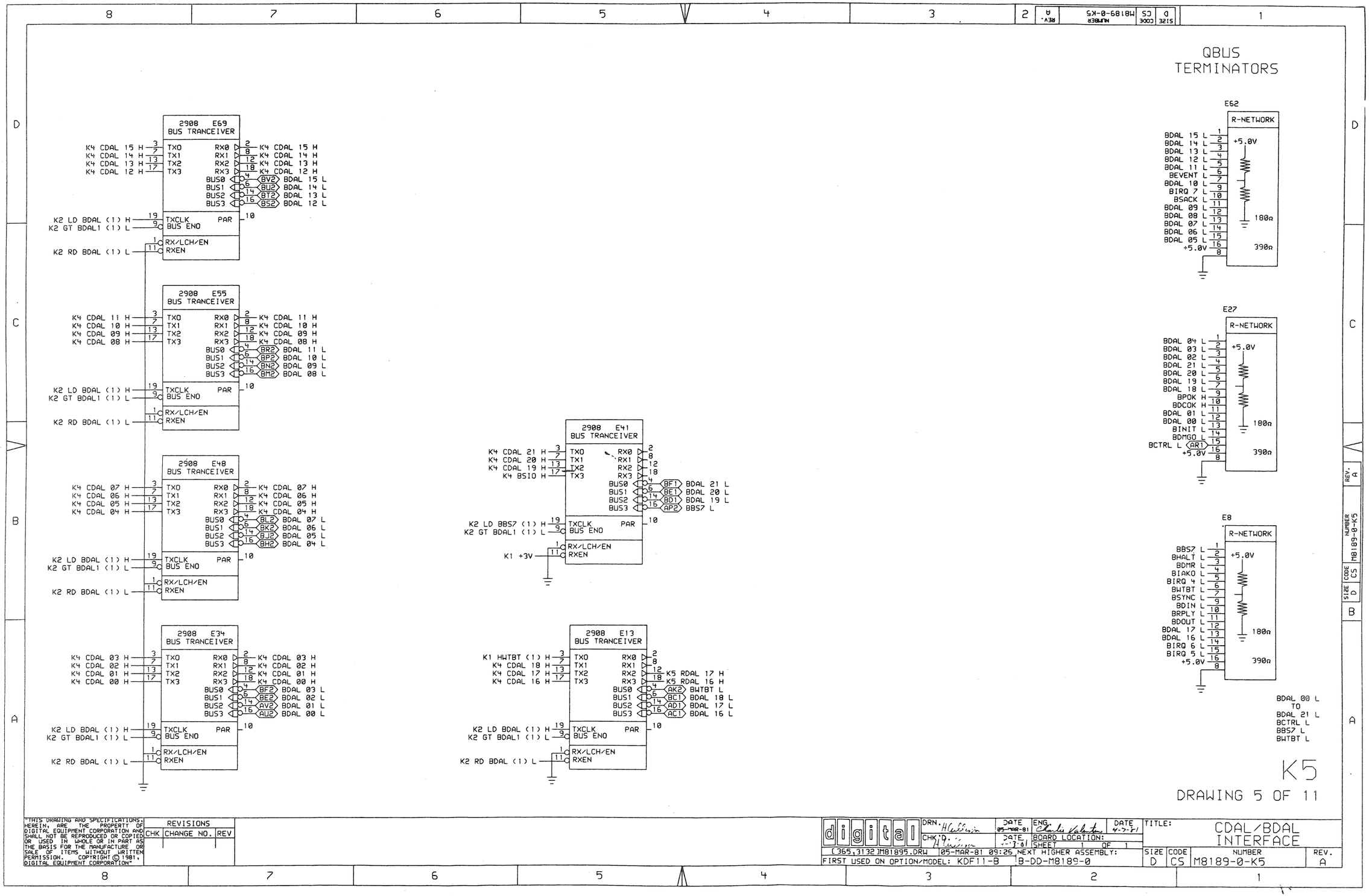
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. [signature] DATE 05-MAR-81 | ENG. [signature] DATE 4-3-81
CHK'D. [signature] DATE 4-1-81 | BOARD LOCATION:
SHEET 1 OF 1
[365,3132]M81894.DRW 05-MAR-81 08:59 | NEXT HIGHER ASSEMBLY: B-DD-M8189-0
FIRST USED ON OPTION/MODEL: KDF11-B

TITLE: F11 CHIPS & FIXED DATA

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K4	A



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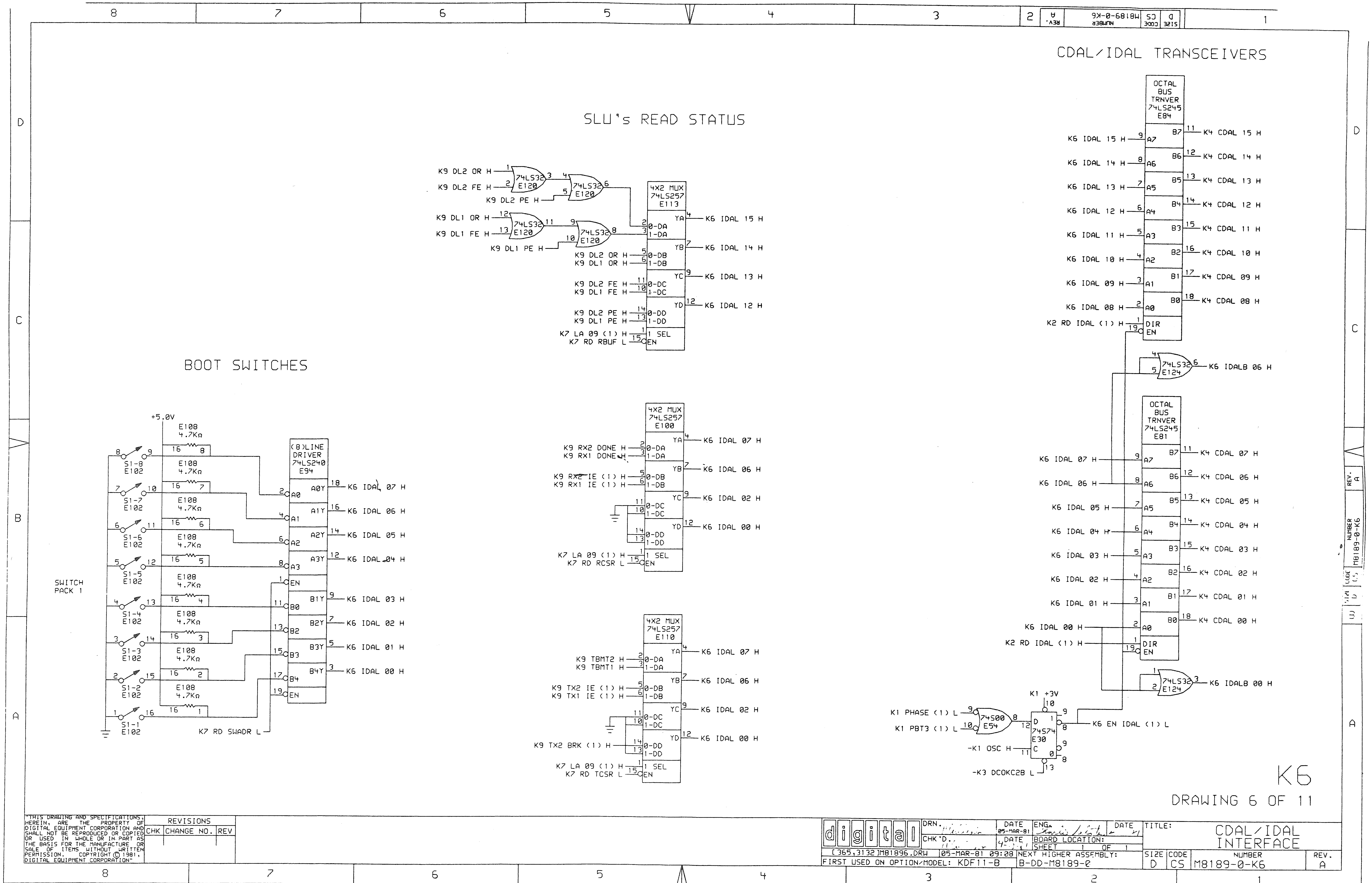
REVISIONS		
CHK	CHANGE NO.	REV

DRN. H Gallagher	DATE 05-MAR-81	ENG. Charles Valentine	DATE 4-7-81	TITLE: CDAL/BDAL INTERFACE
CHK'D. H Gallagher	DATE 4-7-81	BOARD LOCATION: SHEET 1 OF 1		
[365,3132]M81895.DRW 05-MAR-81 09:26		NEXT HIGHER ASSEMBLY:		SIZE D / CODE CS / NUMBER M8189-0-K5 / REV. A
FIRST USED ON OPTION/MODEL: KDF11-B		B-DD-M8189-0		


CDAL/IDAL TRANSCEIVERS
SLU's READ STATUS
BOOT SWITCHES
OCTAL BUS TRNVER 74LS245 E84
OCTAL BUS TRNVER 74LS245 E81
4X2 MUX 74LS257 E113
4X2 MUX 74LS257 E100
4X2 MUX 74LS257 E110
(8)LINE DRIVER 74LS240 E94
74LS32 E120
74LS32 E124
74S00 E54
74S74 E30
+5.0V
E108 4.7KΩ
SWITCH PACK 1
S1-1 E102
S1-2 E102
S1-3 E102
S1-4 E102
S1-5 E102
S1-6 E102
S1-7 E102
S1-8 E102
K9 DL2 OR H
K9 DL2 FE H
K9 DL2 PE H
K9 DL1 OR H
K9 DL1 FE H
K9 DL1 PE H
K7 LA 09 (1) H
K7 RD RBUF L
K7 RD RCSR L
K7 RD TCSR L
K7 RD SWADR L
K9 RX2 DONE H
K9 RX1 DONE H
K9 RX2 IE (1) H
K9 RX1 IE (1) H
K9 TBMT2 H
K9 TBMT1 H
K9 TX2 IE (1) H
K9 TX1 IE (1) H
K9 TX2 BRK (1) H
K6 IDAL 15 H
K6 IDAL 14 H
K6 IDAL 13 H
K6 IDAL 12 H
K6 IDAL 11 H
K6 IDAL 10 H
K6 IDAL 09 H
K6 IDAL 08 H
K6 IDAL 07 H
K6 IDAL 06 H
K6 IDAL 05 H
K6 IDAL 04 H
K6 IDAL 03 H
K6 IDAL 02 H
K6 IDAL 01 H
K6 IDAL 00 H
K4 CDAL 15 H
K4 CDAL 14 H
K4 CDAL 13 H
K4 CDAL 12 H
K4 CDAL 11 H
K4 CDAL 10 H
K4 CDAL 09 H
K4 CDAL 08 H
K4 CDAL 07 H
K4 CDAL 06 H
K4 CDAL 05 H
K4 CDAL 04 H
K4 CDAL 03 H
K4 CDAL 02 H
K4 CDAL 01 H
K4 CDAL 00 H
K2 RD IDAL (1) H
K6 IDALB 06 H
K6 IDALB 00 H
K1 PHASE (1) L
K1 PBT3 (1) L
-K1 OSC H
-K3 DCOKC2B L
K1 +3V
K6 EN IDAL (1) L
K6
DRAWING 6 OF 11
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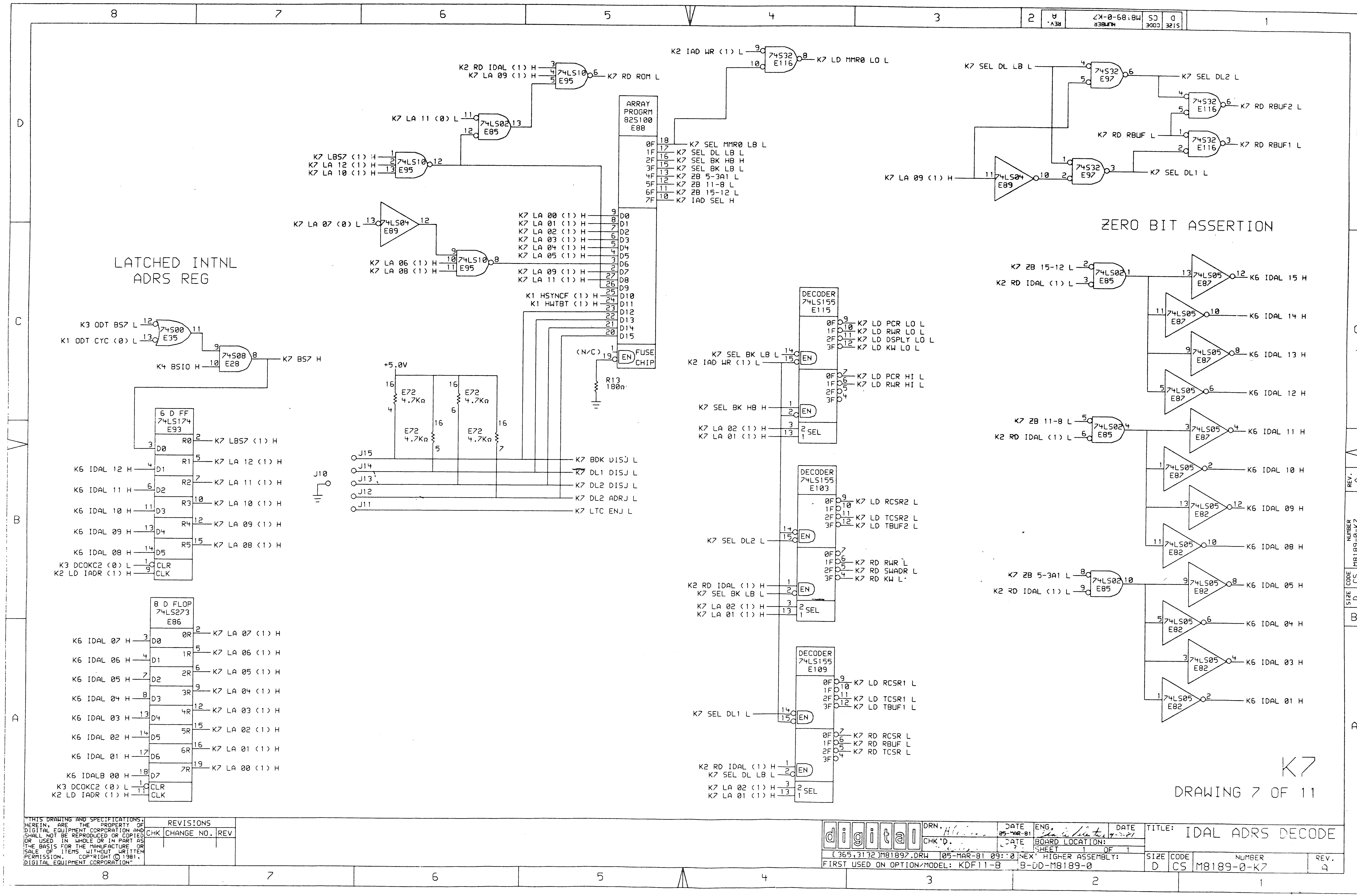
REVISIONS
CHK CHANGE NO. REV
digital
DRN. DATE 05-MAR-81
CHK'D.
ENG.
BOARD LOCATION:
SHEET 1 OF 1
[365,3132]M81896.DRW 05-MAR-81 09:08
NEXT HIGHER ASSEMBLY: B-DD-M8189-0
FIRST USED ON OPTION/MODEL: KDF11-B
TITLE: CDAL/IDAL INTERFACE
SIZE D CODE CS NUMBER M8189-0-K6 REV. A


LATCHED INTNL ADRS REG
ZERO BIT ASSERTION
6 D FF 74LS174 E93
8 D FLOP 74LS273 E86
ARRAY PROGRM 82S100 E88
FUSE CHIP
DECODER 74LS155 E115
DECODER 74LS155 E103
DECODER 74LS155 E109
K7 RD ROM L
K7 LD MMR0 LO L
K7 SEL MMR0 LB L
K7 SEL DL LB L
K7 SEL BK HB H
K7 SEL BK LB L
K7 ZB 5-3A1 L
K7 ZB 11-8 L
K7 ZB 15-12 L
K7 IAD SEL H
K7 SEL DL2 L
K7 RD RBUF2 L
K7 RD RBUF1 L
K7 SEL DL1 L
K7 BS7 H
K7 LD PCR LO L
K7 LD RWR LO L
K7 LD DSPLY LO L
K7 LD KW LO L
K7 LD PCR HI L
K7 LD RWR HI L
K7 LD RCSR2 L
K7 LD TCSR2 L
K7 LD TBUF2 L
K7 RD RWR L
K7 RD SWADR L
K7 RD KW L
K7 LD RCSR1 L
K7 LD TCSR1 L
K7 LD TBUF1 L
K7 RD RCSR L
K7 RD RBUF L
K7 RD TCSR L
K7 BDK DISJ L
K7 DL1 DISJ L
K7 DL2 DISJ L
K7 DL2 ADRJ L
K7 LTC ENJ L
+5.0V
E72 4.7KΩ
R13 180Ω
K6 IDAL 15 H
K6 IDAL 14 H
K6 IDAL 13 H
K6 IDAL 12 H
K6 IDAL 11 H
K6 IDAL 10 H
K6 IDAL 09 H
K6 IDAL 08 H
K6 IDAL 05 H
K6 IDAL 04 H
K6 IDAL 03 H
K6 IDAL 01 H
K7
DRAWING 7 OF 11
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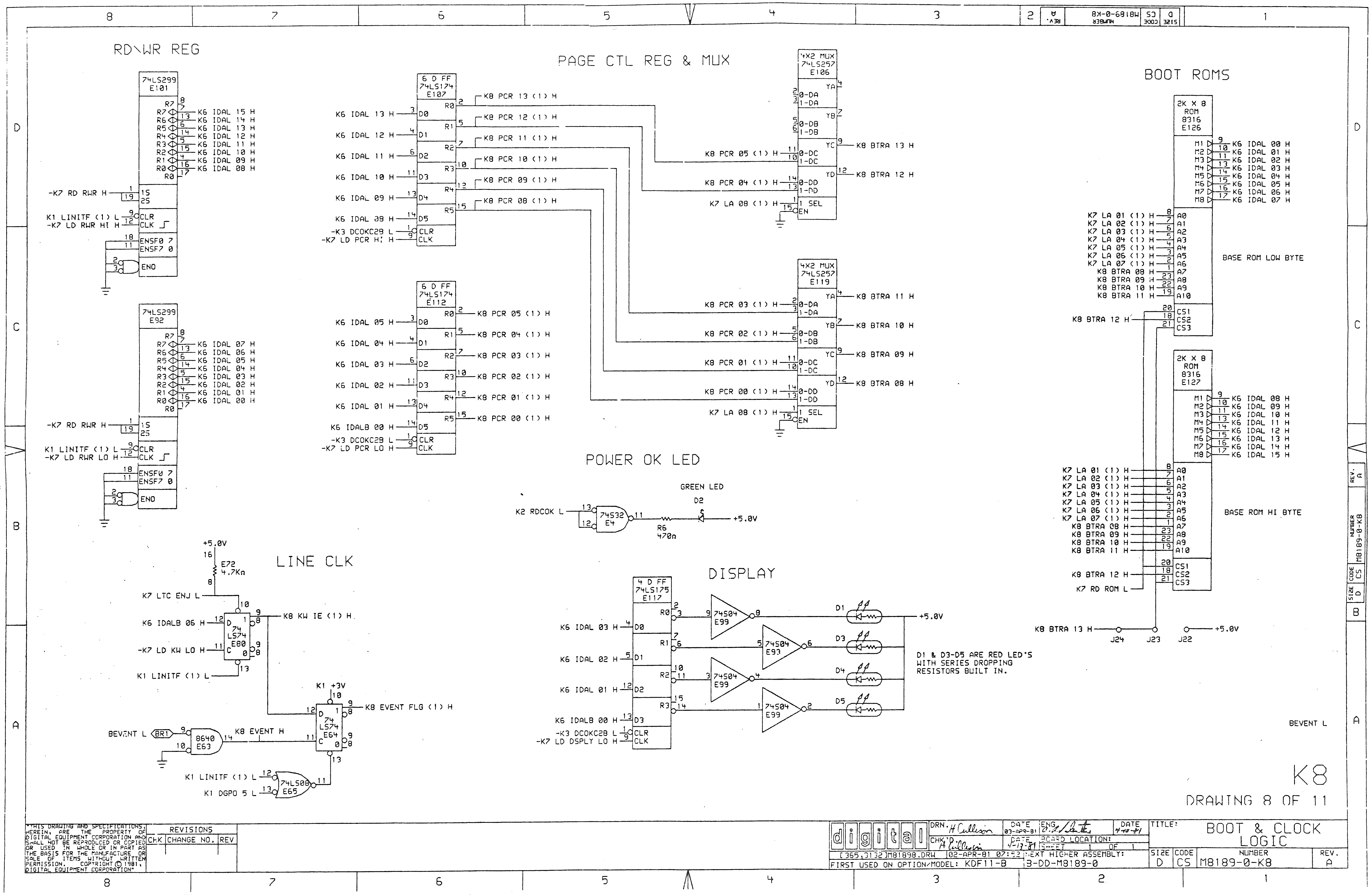
REVISIONS
CHK CHANGE NO. REV
digital
DATE 05-MAR-81
SHEET 1 OF 1
[365,3132]M81897.DRW 05-MAR-81
NEXT HIGHER ASSEMBLY: B-DD-M8189-0
FIRST USED ON OPTION/MODEL: KDF11-B
TITLE: IDAL ADRS DECODE
SIZE D CODE CS NUMBER M8189-0-K7 REV. A


RD\WR REG
74LS299 E101
74LS299 E92
K6 IDAL 15 H
K6 IDAL 14 H
K6 IDAL 13 H
K6 IDAL 12 H
K6 IDAL 11 H
K6 IDAL 10 H
K6 IDAL 09 H
K6 IDAL 08 H
K6 IDAL 07 H
K6 IDAL 06 H
K6 IDAL 05 H
K6 IDAL 04 H
K6 IDAL 03 H
K6 IDAL 02 H
K6 IDAL 01 H
K6 IDAL 00 H
-K7 RD RWR H
K1 LINITF (1) L
-K7 LD RWR HI H
-K7 LD RWR LO H
PAGE CTL REG & MUX
6 D FF 74LS174 E107
6 D FF 74LS174 E112
K8 PCR 13 (1) H
K8 PCR 12 (1) H
K8 PCR 11 (1) H
K8 PCR 10 (1) H
K8 PCR 09 (1) H
K8 PCR 08 (1) H
K8 PCR 05 (1) H
K8 PCR 04 (1) H
K8 PCR 03 (1) H
K8 PCR 02 (1) H
K8 PCR 01 (1) H
K8 PCR 00 (1) H
-K3 DCOKC2B L
-K7 LD PCR HI H
-K7 LD PCR LO H
4X2 MUX 74LS257 E106
4X2 MUX 74LS257 E119
K8 BTRA 13 H
K8 BTRA 12 H
K8 BTRA 11 H
K8 BTRA 10 H
K8 BTRA 09 H
K8 BTRA 08 H
K7 LA 08 (1) H
BOOT ROMS
2K X 8 ROM 8316 E126
2K X 8 ROM 8316 E127
BASE ROM LOW BYTE
BASE ROM HI BYTE
K7 RD ROM L
J24 J23 J22
+5.0V
POWER OK LED
GREEN LED
D2
K2 RDCOK L
74S32 E4
R6 470Ω
LINE CLK
E72 4.7KΩ
K7 LTC ENJ L
K6 IDALB 06 H
-K7 LD KW LO H
K1 LINITF (1) L
K8 KW IE (1) H
74LS74 E80
K8 EVENT FLG (1) H
74LS74 E64
BEVENT L
8640 E63
K8 EVENT H
K1 DGPO 5 L
74LS08 E65
DISPLAY
4 D FF 74LS175 E117
74S04 E99
D1 & D3-D5 ARE RED LED'S WITH SERIES DROPPING RESISTORS BUILT IN.
-K7 LD DSPLY LO H
K8
DRAWING 8 OF 11
BOOT & CLOCK LOGIC
SIZE D CODE CS NUMBER M8189-0-K8 REV. A
FIRST USED ON OPTION/MODEL: KDF11-B
NEXT HIGHER ASSEMBLY: B-DD-M8189-0
02-APR-81
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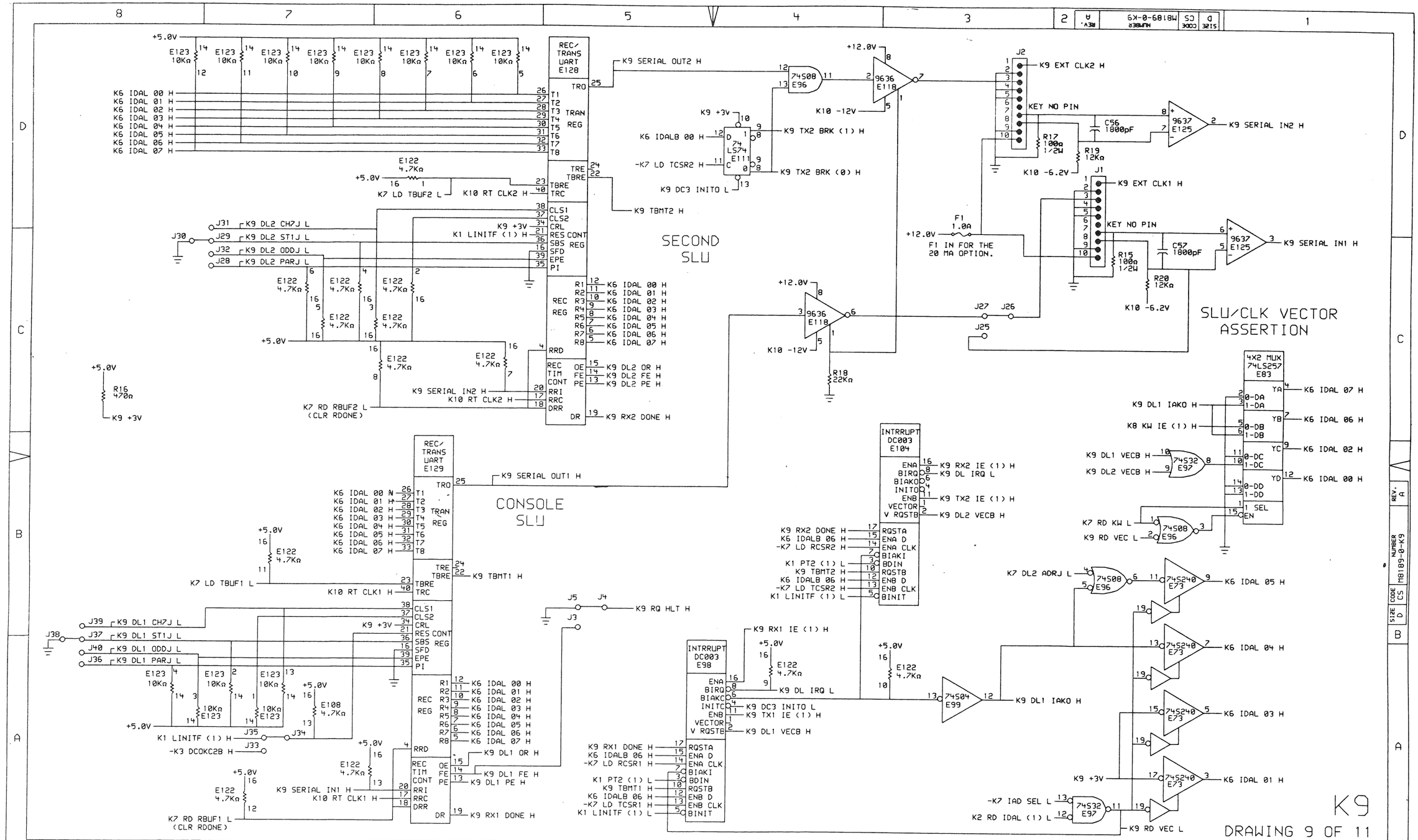
digital


SECOND SLU
CONSOLE SLU
SLU/CLK VECTOR ASSERTION
K9
DRAWING 9 OF 11
REC/ TRANS UART E128
REC/ TRANS UART E129
INTRRUPT DC003 E104
INTRRUPT DC003 E98
4X2 MUX 74LS257 E83
K9 SERIAL OUT2 H
K9 SERIAL OUT1 H
K9 TBMT2 H
K9 TBMT1 H
K9 TX2 BRK (1) H
K9 TX2 BRK (0) H
K9 EXT CLK2 H
K9 EXT CLK1 H
K9 SERIAL IN2 H
K9 SERIAL IN1 H
K9 RX2 DONE H
K9 RX1 DONE H
K9 DL2 OR H
K9 DL2 FE H
K9 DL2 PE H
K9 DL1 OR H
K9 DL1 FE H
K9 DL1 PE H
K9 RQ HLT H
K9 RX2 IE (1) H
K9 DL IRQ L
K9 TX2 IE (1) H
K9 DL2 VECB H
K9 RX1 IE (1) H
K9 DC3 INITO L
K9 TX1 IE (1) H
K9 DL1 VECB H
K9 DL1 IAKO H
K9 RD VEC L
K6 IDAL 00 H
K6 IDAL 01 H
K6 IDAL 02 H
K6 IDAL 03 H
K6 IDAL 04 H
K6 IDAL 05 H
K6 IDAL 06 H
K6 IDAL 07 H
K7 LD TBUF2 L
K10 RT CLK2 H
K7 LD TBUF1 L
K10 RT CLK1 H
K7 RD RBUF2 L (CLR RDONE)
K7 RD RBUF1 L (CLR RDONE)
K1 LINITF (1) H
-K3 DCOKC2B H
K9 DL1 CH7J L
K9 DL1 ST1J L
K9 DL1 ODDJ L
K9 DL1 PARJ L
K9 DL2 CH7J L
K9 DL2 ST1J L
K9 DL2 ODDJ L
K9 DL2 PARJ L
K9 DL1 IAKO H
K8 KW IE (1) H
K9 DL1 VECB H
K9 DL2 VECB H
K7 RD KW L
K7 DL2 ADRJ L
-K7 IAD SEL L
K2 RD IDAL (1) L
K9 +3V
K10 -12V
K10 -6.2V
+12.0V
+5.0V
F1 1.0A
F1 IN FOR THE 20 MA OPTION.
KEY NO PIN
C56 1800pF
C57 1800pF
R17 100Ω 1/2W
R19 12KΩ
R15 100Ω 1/2W
R20 12KΩ
R18 22KΩ
R16 470Ω
E122 4.7KΩ
E123 10KΩ
E108 4.7KΩ
10KΩ E123
74S08 E96
9636 E118
74LS74 E111
9637 E125
74S32 E97
74S04 E99
74S240 E73
DRAWING NUMBER M8189-0-K9
REV. A
SIZE D CODE CS
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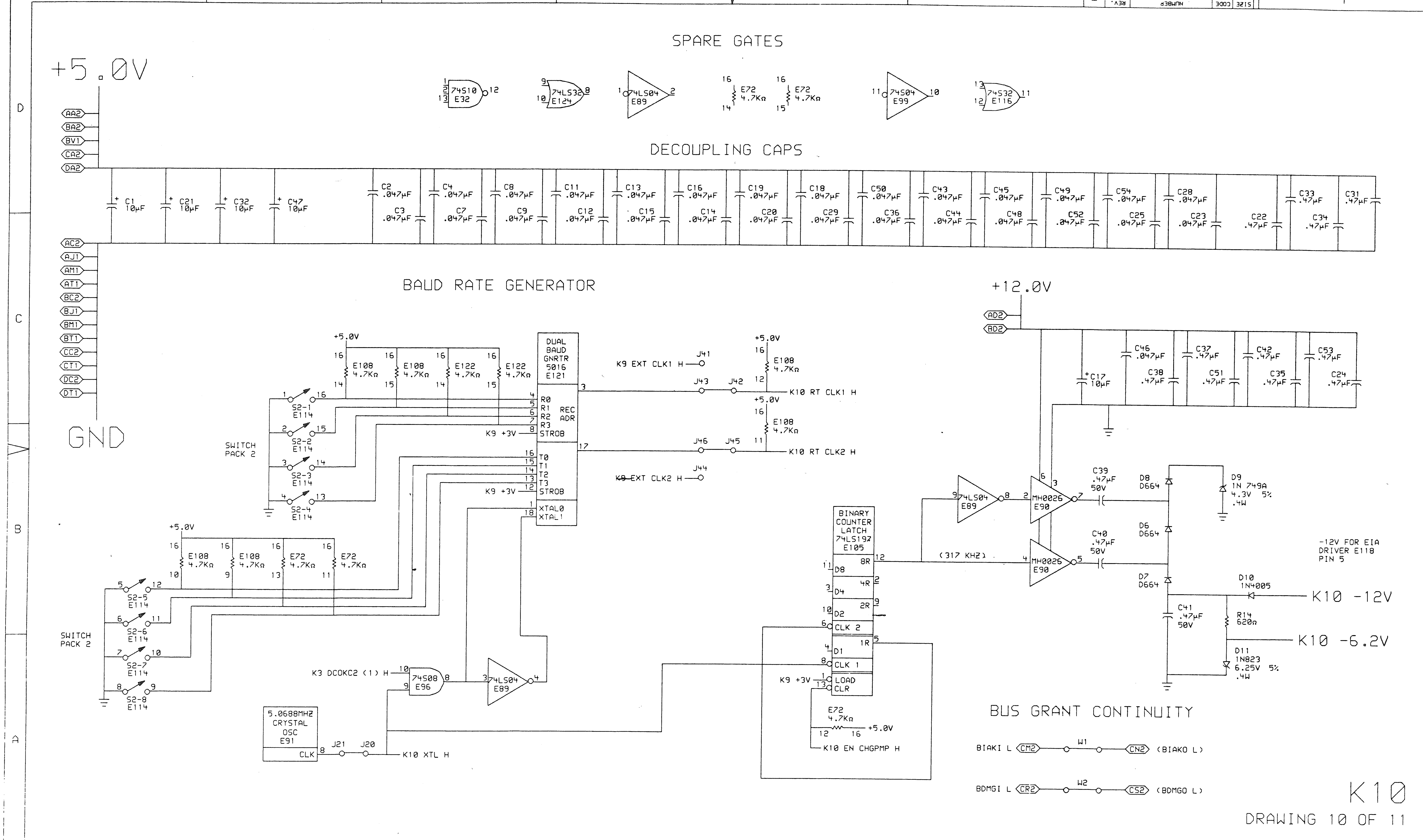
REVISIONS
CHK CHANGE NO. REV
digital
DRN. DATE 05-MAR-81 ENG. DATE 4-7-
CHK DATE 4-13-81 BOARD LOCATION:
SHEET 1 OF 1
[365,3132]M81899.DRW 05-MAR-81 08:04
FIRST USED ON OPTION/MODEL: KDF11-B
NEXT HIGHER ASSEMBLY: B-DD-M8189-0
TITLE: CONSOLE & SECOND SLU
SIZE D CODE CS NUMBER M8189-0-K9 REV. A



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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. DATE 25-MAR-81 | ENG. DATE | CHK DATE
BOARD LOCATION: SHEET 1 OF 1
[365,3132]M81890.DRW 05-MAR-81 20:20
NEXT HIGHER ASSEMBLY: B-DD-M8189-0
FIRST USED ON OPTION/MODEL: KDF11-B

TITLE: BAUD RATE & -12V

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K10	A

CONNECT

J46 TO J45 2ND SLU BAUD RATE SELECTED BY SW. PACK 2 S5-S8 (E114)
J44 TO J45 2ND SLU BAUD RATE DETERMINED BY EXTERNAL SOURCE ON J2 PIN 1

J43 TO J42 CONSOLE BAUD RATE SELECTED BY SW. PACK 2 S1-S4 (E114)
J41 TO J42 CONSOLE BAUD RATE DETERMINED BY EXTERNAL SOURCE ON J1 PIN 1

NOTE: BRG = BAUD RATE GENERATOR

EXT. CLK SOURCE FOR CONSOLE UART
CLOCK INPUT TO CONSOLE UART
CONSOLE BRG OUTPUT

EXT. CLK SOURCE FOR 2ND SLU UART
CLOCK INPUT TO 2ND SLU UART
2ND SLU BRG OUTPUT

J1 J2

PINNING FOR J1 & J2
VIEW LOOKING AT MODULE
FROM THE HANDLE END

SIDE 1 (COMPONENT SIDE)
SIDE 2

NOTE: PIN 6 ON J1 & J2
IS A KEYING PIN (NO PIN)

2ND SLU J2
1ST SLU CONSOLE J1

BAUD RATE GEN. CRYSTAL OSC. OUTPUT 5.0688 MHZ
INPUT TO BAUD RATE GENERATOR
J21
J20

GREEN DC POWER OK LED
ON = DC OK = BDCOK H (BA1) = H
OFF =DC NOT OK

D D D D D
5 4 3 2 1
LSD MSD
BITS 0 1 2 3

J7 BASE TIMING CRYSTAL OSC. OUTPUT 26.666 MHZ
J6 INPUT TO BASE TIMING CIRCUIT

BAUD RATE SELECT

				BAUD RATE
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200
SW# S4	S3	S2	S1	CONSOLE (J1)
SW# S8	S7	S6	S5	2ND SLU (J2)

0 = ON
1 = OFF

BAUD RATE SELECTION TABLE.
SET SWITCHES ON E114
ACCORDING TO TABLE ABOVE.

CONSOLE UART CONFIGURATION J36-J40

GROUND TO SELECT ODD PARITY, OTHERWISE EVEN PARITY. ● J40
GROUND TO SELECT 7 BIT CHARACTERS, OTHERWISE 8 BIT. ● J39
GROUND SOURCE ● J38
GROUND FOR 1 STOP BIT, OTHERWISE 2. ● J37
GROUND TO ENABLE PARITY, OTHERWISE DISABLE. ● J36

SIGNAL OUTPUT K1 LINITF (1) H ● J35
INPUT TO CONSOLE UART RESET E129.21 ● J34
SIGNAL OUTPUT -K3 DCOKC28 H ● J33

J34 CONNECTED TO J35 FOR NORMAL OPERATION, J33 NOT CONNECTED.
J34 CONNECTED TO J33 FOR MANUFACTURING APT TEST ONLY.
J35 NOT CONNECTED.

J27 OUTPUT OF CONSOLE SLU DRIVER
J26 CONSOLE CONNECTOR SLU OUTPUT LINE
J25 CONSOLE SLU INPUT LINE

CONNECT J26 TO J27
FOR NORMAL OPERATION
J25 NOT CONNECTED

CONNECT J26 TO J25
FOR FIELD SERVICE
WRAP AROUND TESTING
J27 NOT CONNECTED.
THIS ALLOWS A TERMINAL
AND ITS CABLE TO BE
CHECKED OUT IN LINE
MODE WITHOUT THE CPU
RUNNING.

2ND SLU UART CONFIGURATION J28-J32

GROUND TO SELECT ODD PARITY, OTHERWISE EVEN PARITY. ● J32
GROUND TO SELECT 7 BIT CHARACTERS, OTHERWISE 8 BIT. ● J31
GROUND SOURCE ● J30
GROUND FOR 1 STOP BIT, OTHERWISE 2. ● J29
GROUND TO ENABLE PARITY, OTHERWISE DISABLE. ● J28

OPTIONAL SOCKET E78 — NOTE: FPF11 MUST PLUG INTO THIS SOCKET IF USED.

OPTIONAL SOCKET E77 — J9, J8

OPTIONAL SOCKET E76

DAT/CTL HYBRID E75

MMU E74

D1,D3,D4 & D5 ARE THE DISPLAY REGISTER INDICATORS
DISPLAY REGISTER ADDRESS = 777524 WRITE ONLY
WRITE A 1 TO TURN OFF A LED
WRITE A 0 TO TURN ON A LED
POWER FAIL OR RESTART (BDCOK H=L) CLEARS THE
REGISTER WHICH TURNS ON ALL 4 LEDS
BITS 15-03 ARE IGNORED

INPUT TO MOS CLOCK DRIVER
OUTPUT K1 PHASE (1) H

NOTE: E75 AND E78 DO NOT HAVE
A .01 UFD CAP CONNECTED TO PIN 1
FOR VBB LIKE E74,E76 AND E77.
THEREFORE YOU CAN NOT INSTALL
DEVICES WHICH REQUIRE THIS CAP.
ONLY HYBRID ASSEMBLIES WITH
INTEGRAL VBB CAPS MAY BE
INSTALLED IN E75 AND E78.

INTERNAL DEVICE ADDRESSES

	ADDRESS	VECTOR
CONSOLE		
RCSR (RECEIVE CSR)	777560	60
RBUF (RECEIVE BUFFER)	777562	
XCSR (TRANSMIT CSR)	777564	64
XBUF (TRANSMIT BUFFER)	777566	
2ND SLU STANDARD ADDRESS J12 NO CONNECTION (H)		
RCSR (RECEIVE CSR)	776500	300
RBUF (RECEIVE BUFFER)	776502	
XCSR (TRANSMIT CSR)	776504	304
XBUF (TRANSMIT BUFFER)	776506	
2ND SLU ALTERNATE ADDRESS J12 GROUNDED (L)		
RCSR (RECEIVE CSR)	776540	340
RBUF (RECEIVE BUFFER)	776542	
XCSR (TRANSMIT CSR)	776544	344
XBUF (TRANSMIT BUFFER)	776546	
BOOT/DIAGNOSTIC REGISTERS		
PAGE CONTROL REGISTER	777520	WO 12 BITS 0-5 & 8-13
READ-WRITE MAINTENANCE REG.	777522	R/W 16 BITS
CONFIGURATION REGISTER	777524	RO 8 BITS 0-7
DISPLAY REGISTER	777524	WO 4 BITS 0-3
BEVENT CSR	777546	100 R/W 1 BIT 6
ROM MEMORY ADDRESSES	773000-773777	
LOW BYTE PCR CONTROLS	773000-773377	
HIGH BYTE PCR CONTROLS	773400-773777	

NOTE: THE INTERNAL DEVICES ARE ADDRESSABLE ONLY BY THE CPU ON THE INTERNAL BUS. THIS INCLUDES ALL MEMORY, MANAGEMENT AND FLOATING POINT REGISTERS. I.E. YOU CANNOT DO A DMA TRANSFER FROM ANY EXTERNAL OPTION TO ANY OF THE INTERNAL DEVICES.

SWITCH PACK 2 (E114) SELECTS BAUD RATE

SWITCH PACK 2 — S1 S2 S3 S4 S5 S6 S7 S8 — E114

SWITCH PACK 1 — S1 S2 S3 S4 S5 S6 S7 S8 — E102

ROM/EPROM SOCKET HIGH BYTE 08-15 E127

ROM/EPROM SOCKET LOW BYTE 00-07 E126

CONFIGURATION REGISTER SWITCH PACK 1 (E102)
8 BITS READ ONLY ADDRESS 777524
BITS 15-08 ALWAYS READ AS 0

SWITCH # S8 S7 S6 S5 S4 S3 S2 S1
DATA BIT 07 06 05 04 03 02 01 00

SWITCH ON = 1
SWITCH OFF = 0

POWER UP MODE SELECTION

MODE	NAME	J19	J17
0	PC @24,PS @26	N/C	N/C
1	CONSOLE ODT	N/C	GND
2	BOOTSTRAP 773000	GND	N/C
3	EXTENDED MICROCODE JUMP TO CONTROL CHIP #37	GND	GND

CONNECT J5 TO J4 FOR NORMAL OPERATION. J3 NOT CONNECTED. FRAMING ERROR (BREAK) FROM CONSOLE IGNORED.

CONNECT J3 TO J4 TO HALT CPU IF BREAK RECEIVED FROM CONSOLE. J5 NOT CONNECTED

J5 GROUND
J4 INPUT K9 RQ HLT H
J3 OUTPUT K9 DL1 FE H

OUTPUT K8 BTRA 13 H
INPUT PIN 21 TO E126 & E127
+5.0V

BUS GRANT CONTINUITY JUMPERS
W2 W1
W1 BIAKO/I
W2 BCNGO/I
W1 & W2 MUST BE INSTALLED WHEN USING A Q/Q BACKPLANE

FOR 2K X 8 EPROMS CONNECT J22 TO J23 WITH J24 NOT CONNECTED

ALL OTHER APPLICATIONS CONNECT J24 TO J23 WITH J22 NOT CONNECTED

J19 SEE POWER UP MODE TABLE ABOVE. PUP CD1J L
J18 GROUND SOURCE
J17 SEE POWER UP MODE TABLE ABOVE. PUP CD0J L
J16 GROUND TO TRAP TO LOC. 10 IF HALT EXECUTED IN KERNEL MODE. OTHERWISE HALT AND ENTER CONSOLE ODT.
J15 GROUND TO DISABLE BOOT/DIAG. ROM & CLOCK LOGIC
J14 GROUND TO DISABLE SLU #1 (CONSOLE)
J13 GROUND TO DISABLE SLU #2
J12 GROUND TO SET SLU #2 REGISTER ADD'S TO 776540/340 OTHERWISE 776500/300
J11 GROUND TO SET THE LINE CLK INTERRUPT ENABLE F/F (BEVENT ALWAYS ENABLED), OTHERWISE BIT 6 OF CSR (777546) CONTROLS F/F.
J10 GROUND SOURCE

NOTE: IF BDV11 IS USED WITH KDF11-B AND BDV11 CONTROLS BEVENT, THEN J15 AND J11 MUST BE GROUNDED.

IF BDV11 IS USED WITH KDF11-B AND BEVENT IS TO BE IGNORED THEN J15 MUST BE GROUNDED BUT NOT J11.

BIT 6 = 1 BEVENT ENABLED IF PSW PRIORITY < 6
BIT 6 = 0 BEVENT DISABLED

BEVENT VECTOR = 100

A A A A A A A A A A A A A A A A A A A A A A
V U T S R P N M L K J H F E D C B A
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

K11
DRAWING 11 OF 11

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REVISIONS		
CHK	CHANGE NO.	REV
P.H.	M1003	B

DRN. P.H. Hebert DATE 03-NOV-83 ENG. DATE
CHK'D. DATE BOARD LOCATION: SHEET 1 OF 1
USRA:<HEBERT>M1189A.DRW 03-NOV-83 13:55 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: KDF11-B B-DD-M8189-0

TITLE: CONFIGURATION GUIDE
SIZE K CODE CS NUMBER M8189-0-K11 REV. B

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NOTE:

FOR FIELD MAINTENANCE PRINT SET REFER TO B-TC-KEF11-BB-1

UNIT VARIATIONS

VAR	TITLE
KEF11-BB	HYBRID C.I.S. MICROCODE CHIP.

REVISIONS		
REV.	A	
CHANGE NO.	INITIAL	
CHK		

USED ON OPTION/MODEL	DRN.	DATE	TITLE
KEF11-BB	A. AMICO	21JAN81	digital DRAWING DIRECTORY KEF11-BB
	CHK'D. ROBICHAUD	DATE 08APR81	
	PROJ. ENG. K. AMUNDSEN	DATE 8 May 81	SIZE B / CODE DD / NUMBEF KEF11-BB / REV A
SHEET 1 OF 2	PROD. Greg. Bylek	DATE 9-Jun-81	DIST.

DRB 106A

MC-3

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
1	MPØ1223-ØØ	KEF11-BB PRINT SET ORDER NO. (MP)	-
	B-TC-KEF11-BB-1	FIELD MAINTENANCE PRINT SET (TC)	-
	K-PL-KEF11-BB-DBP	COMMERCIAL INSTRUCTION SET (KEF11-BB)	E/M
	B-PL-KEF11-BB	SHIPPING LIST KEF11-BB	E/M
2	B-DD-5700006-0	CIS MODULE	E/M
3	A-PS-9905812-0-0	BOX, PAPER SET-UP WITH FOAM	M

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE

TYPE: E ELECTRICAL
M MECHANICAL
E/M ELECTRO/MECHANICAL

digital

TITLE	SHEET	SIZE	CODE	NUMBER	REV
DRAWING DIRECTORY KEF11-BB	2 OF 2	B	DD	KEF11-BB	A

DRB 108A

ML-3