FIELD MAINTENANCE PRINT SET

TABLE OF CONTENTS

UNIT VARIATIONS COVERED BY THIS PRINT SET
AD11-K

208

AD11-K
Field Maintenance Print Set

Digital Equipment Corporation

PRINT SET ORDER NO.
MPØØØ47

REVISIONS		
REV.		
CHG. NO.		
DATE		

USED ON OPTION/MODEL	
AD11-K	
SHEET I OF 1	

DRN.	KW Counter	DATE	[illegible]
CHK'D	Bill Hoyt	DATE	23 FEB 76
PROJ. ENG.	Russ Johnson	DATE	25 FEB 76
FIELD SERV.	B Schofer	DATE	2/23/76

digital

TITLE: AD11-K UNIT ASSY

SIZE	CODE	NUMBER	REV.
B	TC	AD11-K-1	
DIST.			

DRB 124

ENG-0124-16-MTR-(227)

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

SEQUENCE

SEQUENCE

THIS IS PRINT SET

UNIT VARIATIONS		PRINT SET
VAR	TITLE	
AD11-K	AD11-K UNIT ASSY	

REVISIONS		
DATE	CHG. NO.	REV
5-76	AD11-K-1	A
5-76	AD11-K-2	B

DEC-11-ZSI-1-0322-1-A-B-0702

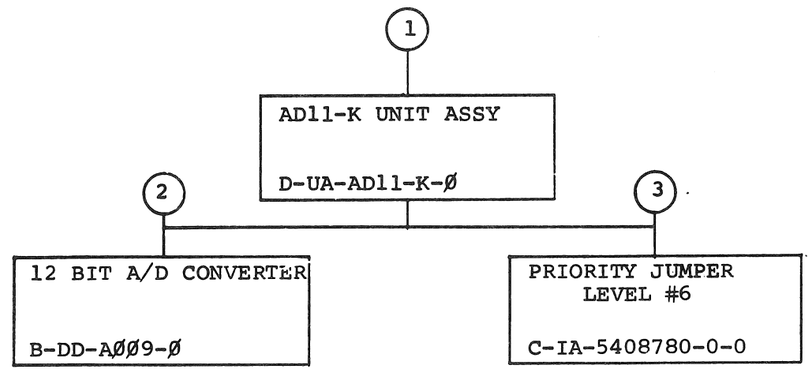
DRB 106

USED ON OPTION/MODEL	
AD11-K	
SHEET 1 OF 3	

DRN.	DATE	TITLE
CHK'D.	DATE	AD11-K UNIT ASSY
PROJ ENG.	DATE	
PROD.	DATE	
FIELD SERV.	DATE	

SIZE	CODE	NUMBER	REV
B	DD	AD11-K	B

DIST



TITLE		SIZE	CODE	NUMBER	REV
AD11-K UNIT ASSY	SHEET 2 OF 3	B	DD	AD11-K	B

DRB 107
DEC 16-(325)--1062—3—N871

ELECTRO/MECHANICAL

CUSTOMER PRINT SET	MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
		1	MPØØØ47	#		AD11-K PRINT SET	
			B-TC-AD11-K-1	#	1	FIELD MAINTENANCE PRINT SET	
			D-UA-AD11-K-Ø	#	1	AD11-K UNIT ASSY	
			A-PL-AD11-K-2	#	1	AD11-K SHIPPING LIST	
			A-SP-AD11-K-3	#	12	AD11-K SPECIFICATION	
			A-SP-AD11-K-4	#	9	AD11-K OPTION CHECKOUT & ACCEPTANCE PROCEDURE	
			A-SP-AD11-K-5	#	14	AD11-K MANUFACTURING + FIELD SYSTEM ACCEPTANCE PROC.	
			A-SP-AD11-K-6	#	6	AD11-K CIRCUIT DESCRIPTION	
			B-DD-AR11-TA	#	2	AR11 BURN IN TESTER	
			B-DD-AR11-TB	#	2	AR11 ANALOG TESTER	
			D-CS-G5Ø36-Ø-1	#	2	WRAP AROUND	
			E-MD-7416528-0-0	#	1	INSULATOR, ANALOG MODULE	
		2	B-DD-AØØ9-Ø	#	2	12 BIT A/D CONVERTER	
		3	C-IA-5408780-0-0	#	1	PRIORITY JUMPER LEVEL #6	
			B-CS-5408780-0-1	#	1	PRIORITY JUMPER LEVEL #6	
			K-CO-5408780-0-4	#	1	X-Y COORDINATE HOLE LOCATION	
			B-MH-5408780-0-5	#	1	MODULE ECO HISTORY	
			C-AH-5408780-0-6	#	1	ASSY/DRILLING HOLE LAYOUT	

CUSTOMER PRINT SET	MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO / FILE DATE

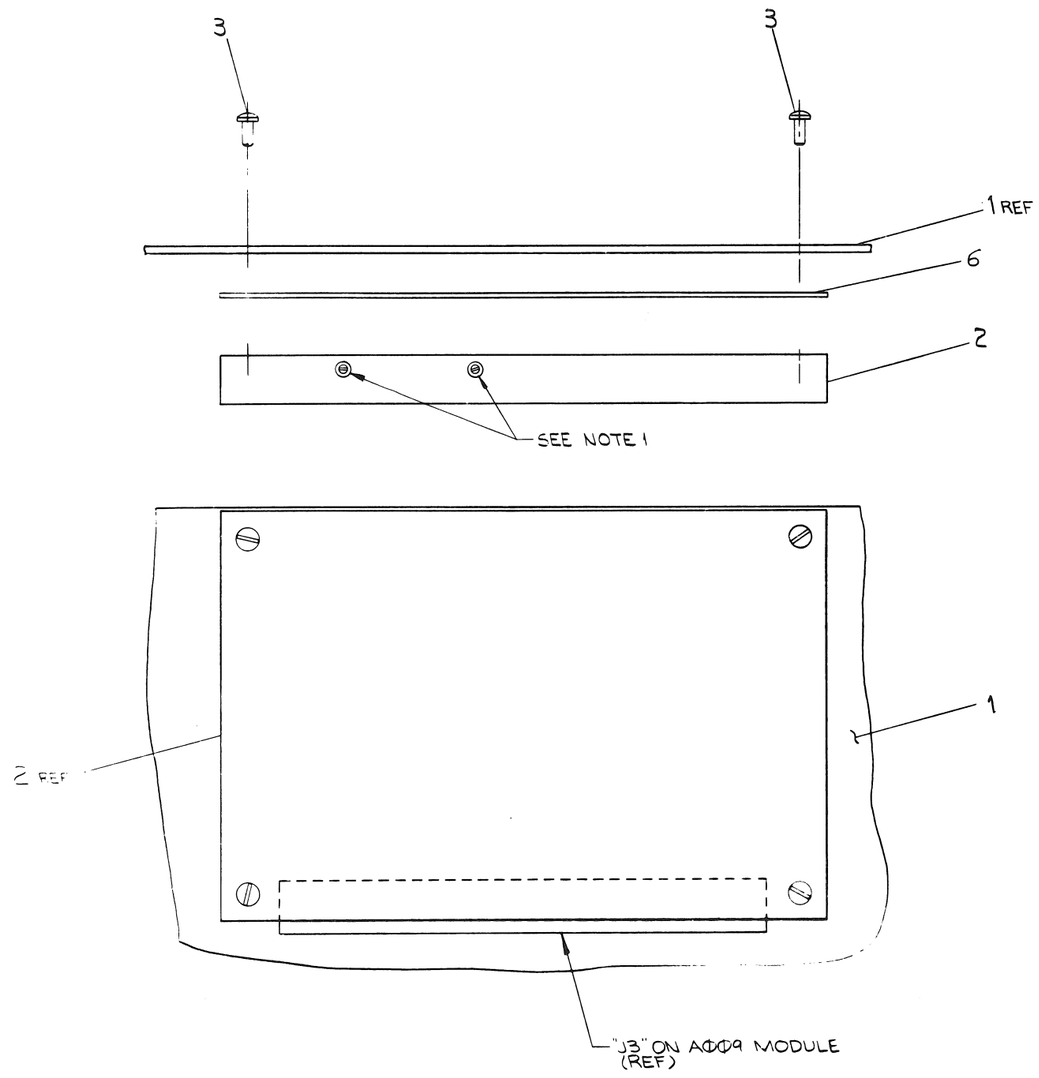
CUSTOMER PRINT SET CODES
X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE	SHEET	SIZE	CODE	NUMBER	REV
AD11-K UNIT ASSY	2 OF 3	B	DD	AD11-K	B

DRB 108

digital EN-01062-2B-16-R972-(325)

NOTES:
1. THESE HOLES ARE FOR OFFSET ADJUSTMENT AND GAIN ADJUSTMENT.
2. ITEMS 4,5,7,8, ARE INCLUDED WITH THIS ASSEMBLY



60	SOCKET CRIMP	1210089-4	8
1	CONN HOUSING LATCH	1210918-15	7
1	INSULATOR ANALOG MODULE	7416528-0-0	6
2	SHIELD QUAD BD. (7.50"x10")	1700021-02	5
2	JUMPER	7010771	4
4	SCR. BINDING HD #4-40x.19	9007650-4	3
1	A/D CONVERTER	3012960-00	2
1	12 BIT A/D CONVERTER	AØØ9	1
	DESCRIPTION	DWG./PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE INCHES: OVER 0 TO 0.2	OVER 0.2 TO 1.2	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 80.0
SURFACE QUALITY IN MICROINCHES	MEDIUM	±.004	±.008	±.012	±.016	±.024	±.04
	PREFERRED	±.012	±.016	±.025	±.04	±.063	±0.1

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL SEE PARTS LIST

FINISH

DRN. R.W. Cavanna 18 DEC 75
CHK'D 14 Jan 76
ENG 25 FEB 76
PROJ. ENG 25 FEB 76
PROD. 25 FEB 76

NEXT HIGHER ASSY. B-DD-ADII-K

SCALE 2/1

SHEET 1 OF 1

FIRST USED ON ADII-K

digital

TITLE ADII-K UNIT ASSY

SIZE	CODE	NUMBER	REV.
D	UA	ADII-K-Ø	A

DIST.

REVISIONS			
CHK.	CHANGE NO.		REV.
	ADII-1		

DEC FORM 825
DRD 1-00-C

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY R. CAUNTER DATE 17 DEC 75	CHECKED Bill Hary DATE 12 JAN 76	SECTION 1
ENG Russ Ohanian DATE 25-FEB-76	PROD R. Walenzuela DATE 25 FEB 76	ISSUED SECT. 1

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION AD11-K
1	MPØØØ47	FIELD MAINTENANCE PRINT SET	1
2	EK-AD11-K-OP-ØØ1	AD11-K USER'S MANUAL	1
3	1700021-Ø2	SHIELD QUAD BOARD (7½" x 10")	2
4	MAINDEC-11-DZADL-D	AD11-K DOCUMENT	1
5	MAINDEC-11-DZADL-PB	AD11-K PAPER TAPE BINARY	1
6	7010771	JUMPER	2
7	D-UA-AD11-K-Ø	AD11-K UNIT ASSY	1
8	MD11-DXADB-A	DEC-X11 AD11-K (KW11-K) EXER	1
9	1210918-15	CONN. HOUSING	1
10	1210089-4	SOCKET CRIMP	60

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV	ECO NO.
AD11-K SHIPPING LIST		A	PL	AD11-K-2	A	AD11-K-00001
	SHEET 1 OF 1	DIST				

DEC FORM DRA 110 DEC 16-(325)-1031-N870

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 5-MAR-76

TITLE AD11-K MANUFACTURING AND FIELD SYSTEM ACCEPTANCE PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	CHANGES ON SH 10 SECT 4	00002	R. IKNAIAN	JULY 76	RBI	6-AUG-76
B	ECO CHANGE	00003	P. TURCOTTE	SEP-76	[illegible]	7-OCT-76
C	ECO CHANGE	MR005	B. AVERY	DEC-77	T Kolen	3-JAN 78

ENG	APPD	SIZE	CODE	NUMBER	REV
Chris Ikhnaian 5-MAR-76	[illegible] 5-MAR-76	A	SP	AD11-K-5	C

DEC 16-(392)-1079-N971
DRA 107

SHT 1 OF 14

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AD11-K MANUFACTURING AND FIELD SYSTEM ACCEPTANCE PROCEDURE

TABLE OF CONTENT

SIZE	CODE	NUMBER	REV
A	SP	AD11-K-5	C

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 2 OF 14

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AD11-K MANUFACTURING AND FIELD SYSTEM ACCEPTANCE PROCEDURE

1.0 SCOPE

This procedure covers the installation and acceptance of an AD11-K in a PDP11 system. It is anticipated that the procedure will be used in one of the following situations:

A. Installation and acceptance of an AD11-K on a PDP11 system in an in-house FA&T system integration area.

B. Add-on installation and acceptance of an AD11-K on an existing PDP11 system in the field.

C. Acceptance of an AD11-K on a new PDP11 system upon installation at a customer site.

D. On-going AD11-K vertification testing at intervals over the life of a given system.

2.0 AD11-K MOUNTING CONFIGURATION CONSIDERATIONS

The AD11-K is a one-module option which interfaces with a PDP11 through an SPC slot. The AD11-K may be mounted in any SPC slot and will operate within specification with no configuration restriction whatsoever regarding physical proximity to processor, memory, or other options. AD11-K analog performance may be further optimized beyond specification levels by mounting in an electrically quiet environment. Consequently, if a choice is available in configuring a system, the AD11-K should be mounted away from the processor and memory modules. Two quad-size electrostatic shields are used to further optimize performance. They are to be placed between the AD11-K and adjacent front and back modules.

SIZE	CODE	NUMBER	REV
A	SP	AD11-K-5	C

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 3 OF 14

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AD11-K MANUFACTURING AND FIELD SYSTEM ACCEPTANCE PROCEDURE

2.1 CABLING

The AD11-K is interfaced to the outside world by means of either a BC20F FOAMED cable to an H322 distribution panel, a BC11-L Berg-to-open end cable, or a user-built cable.

2.2 BUS ADDRESSES

The AD11-K starting address may be set at any address between 160000 and 177740 (in incremements of 40) by means of switches on the module. The preferred starting addresss is 170400. Use of any other starting address will necessitate patches to the AD11-K Diagnostic, as well as to system software (such as RT-11 lab application and SPARTA) which supports the AD11-K. The AD11-K Diagnostic supports multiple AD11-K's automatically, provided that the AD11-K's occupy a sequential block of addresses 40 apart and provided that the address following the last AD11-K is unused. For example, in a system with a single AD11-K at 170400, the address 170440 should not be used; a system with three AD11-K's should have the AD11-K's at 170400, 170440 and 170500, with the address 170540 unused.

2.3 VECTORS

The AD11-K vector space may start in increments of 40 up to a maximum of 740 by means of switches on the module. The preferred vector is 340. Use of any other vector will necessitate patches to the AD11-K Diagnostic, as well as to system software which supports the AD11-K. For the AD11-K diagnostic to work properly with multiple AD11-K's in a system, the AD11-K vectors should be in sequential order, 40 apart. For example, in a system with

SIZE	CODE	NUMBER	REV
A	SP	AD11-K-5	C

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 4 OF 14

three AD11-K's at 170400, 170440 and 170500, the vectors should be 340, 400 and 440 respectively

3.0 EQUIPMENT REQUIRED

1. Oscilloscope
2. BG5036 maintenance kit. (G5036 wraparound module and a BC08R-1 cable).
3. Calibrated DC voltage source (EDC model MV 116 or equivalent). Two are needed if a wraparound module is not available.

4.0 DIAGNOSTICS

There are two diagnostic to be used in the acceptance of the AD11-K, AD11-K Diagnostic (MAINDEC-11-DZADL-A) and AD11-K DEC-X11 System Exerciser module (MD11-DXADB-A). The AD11-K diagnostic is to be used for the operational verification of the AD11-K and to trouble-shoot any problem encountered with the AD11-K. The AD11-K DEC-X11 is used to verify the system operation with an AD11-K.

4.1 AD11-K DIAGNOSTIC (MAINDEC-11-DZADL-A)

This diagnostic is used for checkout, calibration and acceptance of an AD11-K option. It consist of 6 subtest each with a letter code identity (see table 1). After starting at address 200 a listing of each subtest and letter code is printed. It is important that the 200 starting address be used because the test limits are automatically set for system level testing. The subtest letter plus a carriage return is used to enter a test, a Control C is used to exit a test and a Control A is used to return to the beginning of a test. This test should be used to trouble-shoot any hardware failures that may occur.

A - AUTO TEST
C - CALIBRATION
L - LOGIC TEST
N - NOISE TEST
S - SETTLE TEST
W - WRAPAROUND TEST

TABLE 1: AD11-K SUBTEST

The Auto Test consist of a logic test, noise test, an interchannel settling test and a differential linearity test. This test is used if a wraparound module (G5036) is connected to J1.

Calibration Test is used to adjust the offset and gain. A voltage source (EDC) must be attached to an input (specified in switch register bits 5-Ø). Converted values are continually printed as the adjustments are being made. The wraparound module is not necessary in this test. The wraparound module can be used for inputting a voltage into channel Ø via the split lugs.

The logic test is used to test and trouble-shoot the logic portion of the AD11-K. This test checks that a conversion can be done, the data is disregarded. The wraparound is not needed to run this test.

Noise test is used to test for the amount of noise on an A/D channel. This test is used if a wraparound module is not available (for example for testing by a customer who has not purchased the BG5036 option). A voltage must be supplied to the selected input channel.

The Interchannel Settling Test is used to test the A/D for the accuracy of settling to an input channel. This test is used if a wraparound module is not available. Two voltages must be supplied to two selected input channels.

4.2 AD11-K DEC-X11 SYSTEM EXERCISER MODULE (MD11-DXADB-A)

The DEC-X11 System Exerciser is used to test the AD11-K in a system environment. The AD11-K DEC-X11 module can initiate conversion either by program starts or, if a KW11-K is present in the system, by clock overflows.

In order to run the AD11-K DEC-X11 module with a KW11-K for its clock overflow, the KW11-K DEC-X11 module must be disabled from running and the AD11-K DEC-X11 module must be selected to start the KW11-K

5.0 AD11-K INSTALLATION PROCEDURE

Based on the considerations in section 2, choose any SPC mounting slot, starting address and vector for the AD11-K to be installed as follows:

1. Set up the base address of the AD11-K by using figure 1. Switch "On" is set for a Ø and "Off" for a 1.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
			S2-10	S2-9	S2-8	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1	S3-8	LOGICALLY DECODED	
			SWITCH SELECTABLE												

Figure 1: AD11-K ADDRESS SELCTION

For example, to set up for address 170400, bits 2,3,4,5,6,7,9,10,11 switches are set "On" and bits 8 and 12 switches are set "Off".

2. Set up the vector address of the AD11-K by using figure 2. Switch "On" is for a 1 and "Off" for a Ø.

8	7	6	5	4	3	2	1	0
S3-6	S3-5	S3-4	S3-3	S3-2	S3-1	NOT SELECTABLE		
SWITCH SELECTABLE								

Figure 2: AD11-K VECTOR SELECTION

For example, to set up the AD11-K to 340, bits 7,6 and 5 switches are "On" and bits 8,4 and 3 switches are "Off".

3. Set S1 on the AD11-K to switch position 1 (single-ended inputting).

4. Install the AD11-K module in the selected SPC slot.

5. If the system includes an H322 signal distribution panel, connect the AD11-K to the H322 by means of a BC20F Berg-to-Berg cable. When and if the wraparound module is used in the acceptance of the AD11-K, it is acceptable to connect the wraparound module at the H322's end of the BC08R. If the system includes a BC11-L Berg-to-open end cable, do not install the cable at this time. Instead install the BC08R-Ø cable which is to be used with the G5036 wraparound module for acceptance testing. The BC11L is to be installed at the completion of the acceptance testing.

6. Install the electromagnetic shields on both sides of the AD11-K

7. Conduct an acceptance test per section 6.

6.0 AD11-K ACCEPTANCE

This section contains two procedures. One is for use by manufacturing acceptance, QC acceptance and field acceptance (if a G5036 wraparound module is available). This is the preferred method for acceptance of an AD11-K. The second procedure is for field acceptance when a wraparound module is not available (or the customer does not have the BG5036 maintenance option).

6.1 ACCEPTANCE PROCEDURE IF WRAPAROUND IS AVAILABLE

1. Install the G5036. IMPORTANT NOTE: THE BC08R-01 cable should be connected "upside-down" at the G5036 end, i.e, A to VV rather than A to A, and "right-side up" at the AD11-K end, i.e, A to A.

2. Set the switch on the G5036 module to the "E" position. Connect the EDC voltage source signal output to the "E" split lug on the G5036. Connect the EDC voltage source return to the "G" split lug on the G5036. The EDC should be floating* to avoid ground loops. The EDC leads should be short and shielded if possible. The EDC output is now connected to the AD11-K A/D channel 0 input.

3. Load the AD11-K Diagnostic and run Calibration Test (subtest C). Set the EDC to +1.22mV (to check the offset). The printouts should be 4000 and 4001, 50% (±20%) of each out of three consecutive lines of conversion printouts. Make adjustments if necessary, refer to Calibration section 8.1.

* CAUTION: The case on a floating instrument may rise to line voltage if a fault in its primary wiring exists.

4. Remove the EDC and place the G5036 switch to position "0". Run Auto Test, subtest A, for two non-erroring passes. If relative accuracy test failed, run a third pass which must be non-erroring.

5. Load DEC-X11 System Exerciser with the AD11-K exerciser module (MD11-DXADB-A). Run this for a minimum of 15 minutes. This step may be performed at the end of FA&T system checkout. Refer to section 7, if a KW11-K is present.

6. Remove the G5036 wraparound module. It is not shipped with the AD11-K.

7. If the system includes an H322 distribution panel, reconnect the BC20F cable to the H322. If the system does not include an H322, remove the BC08R-01 cable which belong with the G5036. It is not shipped.

8. If the system includes a BC11-L cable, it should be installed at this time.

9. Verify that all items on the AD11-K shipping list (A-PL-AD11-K) are present and properly packed for shipment.

6.2 ACCEPTANCE PROCEDURE IF WRAPAROUND IS NOT AVAILABLE

1. Connect the EDC voltage source signal output to an A/D input (Channel 0 is pin VV of J1). Connect the EDC voltage source return to an analog ground (pins KK,EE,AA or W of J1). The EDC should be floating to avoid ground loops. The EDC leads should be short and shielded if possible.

2. Load the AD11-K Diagnostic and run Calibration Test (subtest C). Set the EDC to +1.22mV (to check the offset). The printouts should be 4000 and 4001, 50% (±20%) of each out of three consecutive lines of conversion printouts. Make adjustments if necessary,

refer to Calibration section 8.1.

3. Connect the EDC voltage source signal output to an A/D input channel 16 (pin N of J1). Set the EDC to ±5V. Connect another EDC voltage source output to an A/D input channel 15 (pin R of J1). Set the EDC to -5V. The EDC returns should be connected to analog ground (pins KK,EE,AA, or W of J1). Both EDC's should be floating to avoid ground loops. Any two A/D channels may be used if you do not want to use 15 and 16.

4. Run Settle Test, subtest S. The diagnostic will ask for the channel numbers being used. The results are printed for each pass. If an error occurs, it will be reported. This test should run for a minimum of two passes.

5. Run Noise Test, subtest N. The diagnostic will ask for the channel number being used. Use one of the A/D channels from step 4. The results are printed for each pass and if an error occurs, it will be reported. This test should run for a minimum of two passes.

6. Remove the EDC's. Run Logic Test, subtest L, for 10 mins.

7. Load DEC-X11 with the AD11-K exerciser module. Run this for a minimum of 15 minutes. Refer to section 7, if a KW11-K is present.

8. If the system includes an H322 distribution panel, reconnect the BC20F cable between the AD11-K (J1) and H322.

9. If the system includes a BC11-L cable it should be installed at this time.

10. Verify that all items on the AD11-K shipping list are included and packaged.

7.0 AD11-K INSTALLED WITH A KW11-K

The KW11-K is a dual programmable real time clock. The Overflow or Schmitt Trigger of one of the clocks (Clock A) can be used to start an A/D conversion. This allows the A/D conversions to operate asynchronous to the Unibus, which will enable the diagnostic to measure the effect of noise from the Unibus into the A/D. The KW11-K module (M7025) should be mounted close to the AD11-K module. The 7010771 jumpers included with the AD11-K, are used to connect tab 1 of the AD11-K to Tab 1 of the KW11-K. Do not connect Tab 2 of the AD11-K to Tab 2 of the KW11-K at this time. Run DEC-X11 System Exerciser with the AD11-K and KW11-K (MD11-DXKWD-A) exerciser modules. Disable the KW11-K exerciser module and select the AD11-K exerciser module to start the KW11-K. Connect Tab 2 of the AD11-K to Tab 2 of the KW11-K after completion of the DEC-X11 System Exerciser.

8.0 CALIBRATION

1. Connect an EDC voltage source signal output to an A/D input channel (channel 0 is pin VV of J1). Connect the EDC voltage source return to an analog ground (pins KK,EE,AA or W of J1). The EDC should be floating to avoid ground loops.

2. Load the AD11-K Diagnostic and run Calibration Test, subtest C, with the A/D channel under test selected in switch register bits 5-0.

3. Set the EDC to +1.22mV. Adjust the offset for printouts of 4000 and 4001, 50% (±20%) of each of three consecutive lines of printouts.

4. Set the EDC to +4.99634V. Adjust the gain for printouts of 7776 and 7777, 50% (±20%) of each of three consecutive lines of printouts.

5. Set the EDC to +1.22mV. The printouts should still be 4000 and 4001. If not repeat steps 3 and 4.

6. Remove the EDC. The A/D is now calibrated

8.2 NON-STANDARD CALIBRATION

The AD11-K is standardly set up for a ±5V input range. There are other input ranges which the user may choose to operate, ±5.12V, ±10V, ±10.24V, 0 to +10V and 0 to +10.24V. The optional ranges are selected by solder jumpers W1 (A or B), W2 (A or B) and W4 (refer to manual EK-AD11K-OP-001). The calibration procedure is the same as in section 8.2 except for the EDC voltages and printouts of the converted values. Refer to table 2 for the correct EDC voltages and conversion values.

RANGE	EDC INPUT VOLTAGE	CONVERTED VALUE 50% EACH ±20%	
±5V	+1.22 mV	4000/4001	
±5.12V	+1.25 mV	4000/4001	FOR
0-10V	+1.22 mV	0000/0001	OFFSET
0-10.24V	+1.25 mV	0000/0001	ADJUSTMENT
±10V	+2.44 mV	4000/4001	
±10.24V	+2.50 mV	4000/4001	
± 5V	+4.99634V	7776/7777	
±5.12V	+5.11625V	7776/7777	FOR
0-10V	+9.99634V	7776/7777	GAIN
0-10.24V	+10.23625V	7776/7777	ADJUSTMENT
±10V	+9.99268V	7776/7777	
±10.24V	+10.23250V	7776/7777	

TABLE 2: NON-STANDARD CALIBRATION VALUES

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 11-MAR-76

TITLE AD11-K CIRCUIT DESCRIPTION

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
Russ Ohmsen 11-MAR-76		A	SP	AD11-K-6	

DEC 16-(352)-1079-N971
DRA 107

SHT 1 OF 6

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AD11-K CIRCUIT DESCRIPTION

The AD11-K is a 16 channel 12-bit analog to digital (A/D) converter. It consists of an A009 quad size module and an A/D converter package. The A009 module circuits consist of a Unibus interface, an 8-bit digital to analog converter (DAC), a linear ramp generator, a DC to DC converter power supply, and associated logic for the A/D converter package. The A/D converter package contains a 16-channel analog multiplexer, a sample & hold, a successive approximation A/D converter and associated circuitry.

The circuits to be described are referenced to print D-CS-A009-0-1, which consists of six sheets. Each sheet has a name description and an alpha-numeric identification (DØ to D5). All signals are source prefixed with the alpha-numeric identification. For example; signal DØ LD STAT HI L (load status register high byte) is generated on sheet DØ which is titled Bus Address Select.

It is assumed the reader is familiar with Unibus operation and is familiar with interpreting circuit schematics of logic and circuits so that a detailed description is not necessary. The description given here is to familiarize the user with the AD11-K circuits enough to identify a portion needing attention. It is recommended that the user read the AD11-K manual EK-AD11K-OP-001).

The Unibus interface consists of the device address decoding, interrupt logic and arbitration, and the Unibus signal receivers and drivers. The bus address lines are received and gated with BUS MSYN (Master Sync) to decode DØ DEV ENABLE (sheet DØ). Address lines 2 through 12 are X-OR'ed with switches.

SIZE	CODE	NUMBER	REV
A	SP	AD11-K-6	

DEC FORM NO EN-01022-16-N370-(381)
DRA 108

SHEET 2 OF 6

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AD11-K CIRCUIT DESCRIPTION

This gives the capability of changing the base device address to avoid address conflicts with other options or AD11-K's. Device Enable is then gated with address line A1 for device register selection (buffer or status register), and AØ for upper or lower byte selection, and the "C" lines.

The interrupt logic and arbitration is located on the upper left of sheet D1. When the done flag is set by D1 EOCP 2 (end of conversion pulse two) and if D1 INTR ENB flop is set, an interrupt is generated by the 8647 (E36) IC onto the Bus Request line. Since it is this device that is requesting the interrupt, the 8647 will not pass the Bus Grant. When bus grant occurs (D1 BG IN), Bus Sack is sent and D1 BBSY (Bus Busy) is set. The Bus Request is taken off the Unibus and Bus INTR and the vector lines are put onto the Unibus. The vector address is switch selectable to avoid conflicts with other devices. When the CP accepts the vector addressing, it sends a BUS SSYN (slave sync) which clears the done flag and D1 BBSY. When BBSY is cleared, BUS INTR and the vector lines are taken off the Unibus.

The Bus Data line receivers and drivers are on sheet D2. The A/D buffer and status register are read registers and are multiplexed onto the data bus depending on the device register being addressed.

The 8-bit digital to analog converter is located on the left side of sheet D4. The circuit consist of an 8-bit holding register preset to $200_{(8)}$ the DAC (MC1408) and a 741 op-amp to amplify the DAC output to ±1.8V.

SIZE	CODE	NUMBER	REV
A	SP	AD11-K-6	

DEC FORM NO EN-01022-16-N370-(381)
DRA 108

SHEET 3 OF 6

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AD11-K CIRCUIT DESCRIPTION

When the wrap-around module (G5036) is connected, the DAC outputs (D4 DAC OUTPUT, D4 TEST CH15 and D4 TEST CH16) are connected to A/D inputs (input 7, 15 and 16). This allows the A/D to be programmably tested to 3/50'th of an LSB (1LSB = 2.44MV) for relative accuracy and state width.

The linear ramp generator is located on the right side of sheet D4. The circuit is a square wave oscillator with an integrated output (741 op-amp) to produce a linear ±8.5V ramp putput. When the wrap-around module is used (G5036) the ramp output is connected to an A/D input (channel 11). When the DAC and ramp generator are used together, the A/D can be, under program control, tested for relative accuracy, linear differentiality, and state width.

A DC to DC converter, located at the middle top of sheet D3, is used to convert +5VDC to ±15VDC.

The A/D converter is located on sheet D3. The analog multiplexing, sample and hold, and the successive approximation A/D converter circuitry is contained in this package (E24). The output digital data is stored in a 12-bit buffer which is located at the end of a conversion cycle. S1, which is a double pole 5-position rotary switch, is used to setup the A/D package for differential or single-ended usage. When S1 is in any position other than position one, (or position 6) the A/D is setup for differential usage. Both HI MUX (E24-18T) and LO MUX (E24-17B) are held true which forces the package to use inputs 0+1, 2+3 etc., as paired inputs. Q7 is off, allowing MUX OUT LO (E24-11B) to be used as a signal return to AMP IN LO (E24-12B).

SIZE	CODE	NUMBER	REV
A	SP	AD11-K-6	

DEC FORM NO EN-01022-16-N370-(381)
DRA 108

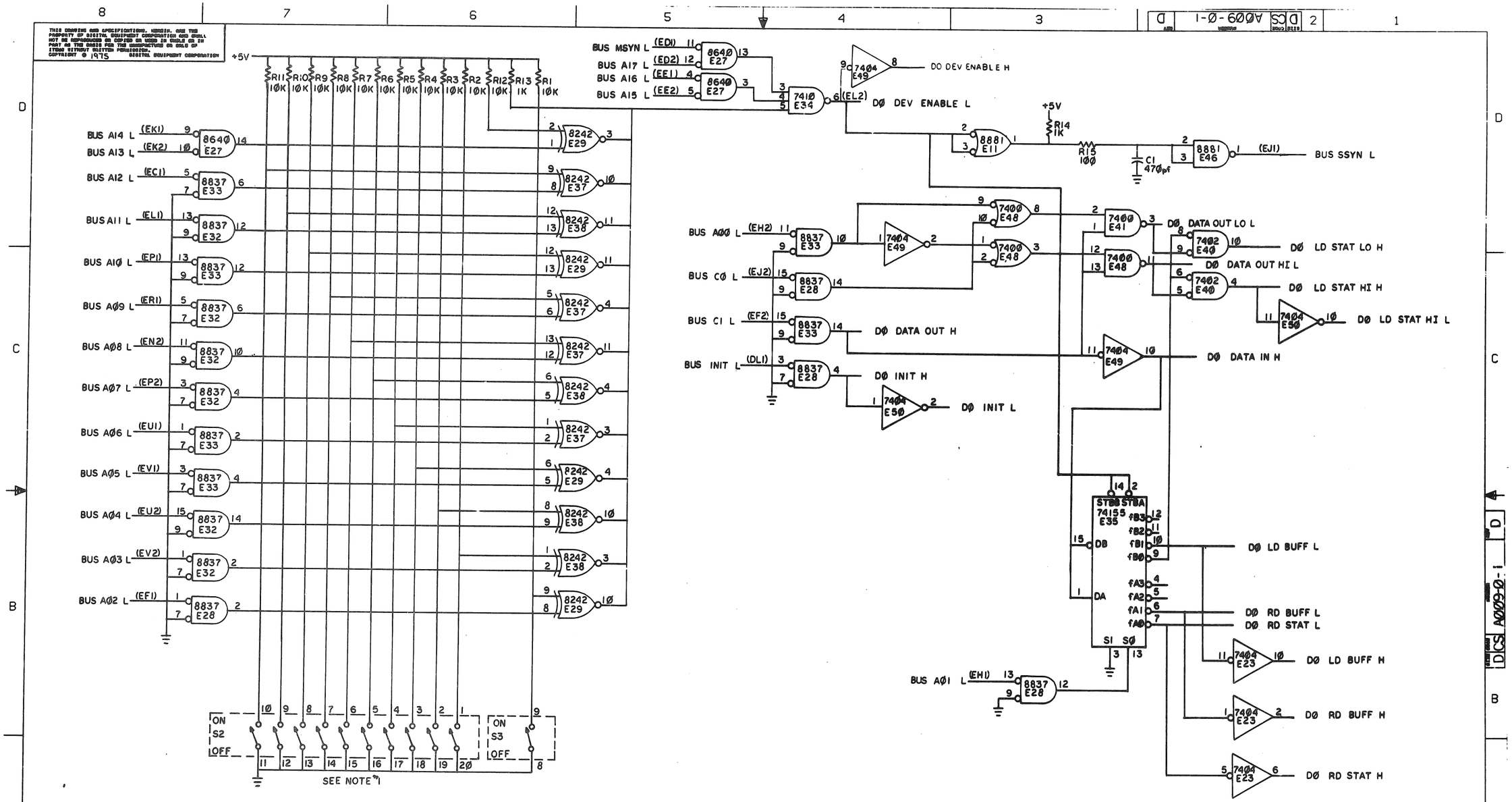
SHEET 4 OF 6

This return is the second leg of the paired inputs (1,3,4 or 5). When S1 is in position one (note that S1 repeats twice each revolution), the A/D is setup for single ended operation. Here the A/D package accepts the input from any of the 16 input channels. The return is enabled by Q7 to MUX IN LO (E24-12B). The return in this case is common to all 16 channels. Q4 and associated circuit is used for external expansion channels 20-77 (lower right of D3). To initialize the A/D package an enable is needed (E24-25B). Initialize is used as the enable and its leading edge is delay by an RC circuit and used as the package initialization. For the jumper configuration refer to the user manual.

The multiplexer bits Ø to 3 are contained in the A/D package. Bits 4 and 5 are located on sheet D1, along with the rest of the status register.

The circuit used to start an A/D conversion is located on sheet D1. There are three methods in starting an A/D conversion, by program starts, clock overflows, or by external starts. The program start is delayed to allow for the channel multiplexer to settle to the respective selected channel. When channels 0-17 are selected, a 10µsec delay is used. Both the external and program starts are received into a 100nsec one shot pulse shaper. D1 AD START flip flop is used to start the A/D package into a conversion cycle. It is cleared at the end of the conversion cycle (from 5 to 15µsec depending on the A/D package).

The error circuitry is located at the top of sheet D1. The error flag is set by two methods, when a second conversion is started before a previous conversion is completed or when an end of conversion occurs before the data buffer is read from a previous conversion. The flip flop, E47-8/9 is set when a conversion is in progress and a second A/D start is given. The error flag will not set until the conversion cycle is completed. D1 SAVE flip flop is used to remember that there is data in the buffer. If a second conversion ends before the data buffer is read the error flag will set.



NOTES: 1. ADDRESS SWITCH SETTINGS:
OFF FOR A LOGIC "1"
ON FOR A LOGIC "0"

CHK	CHANGE NO	REV
X	ORIGINATED	A
	A009-000011	B
	A009-000021	C
	A009-000004	D

BUS ADDRESS SELECT DØ

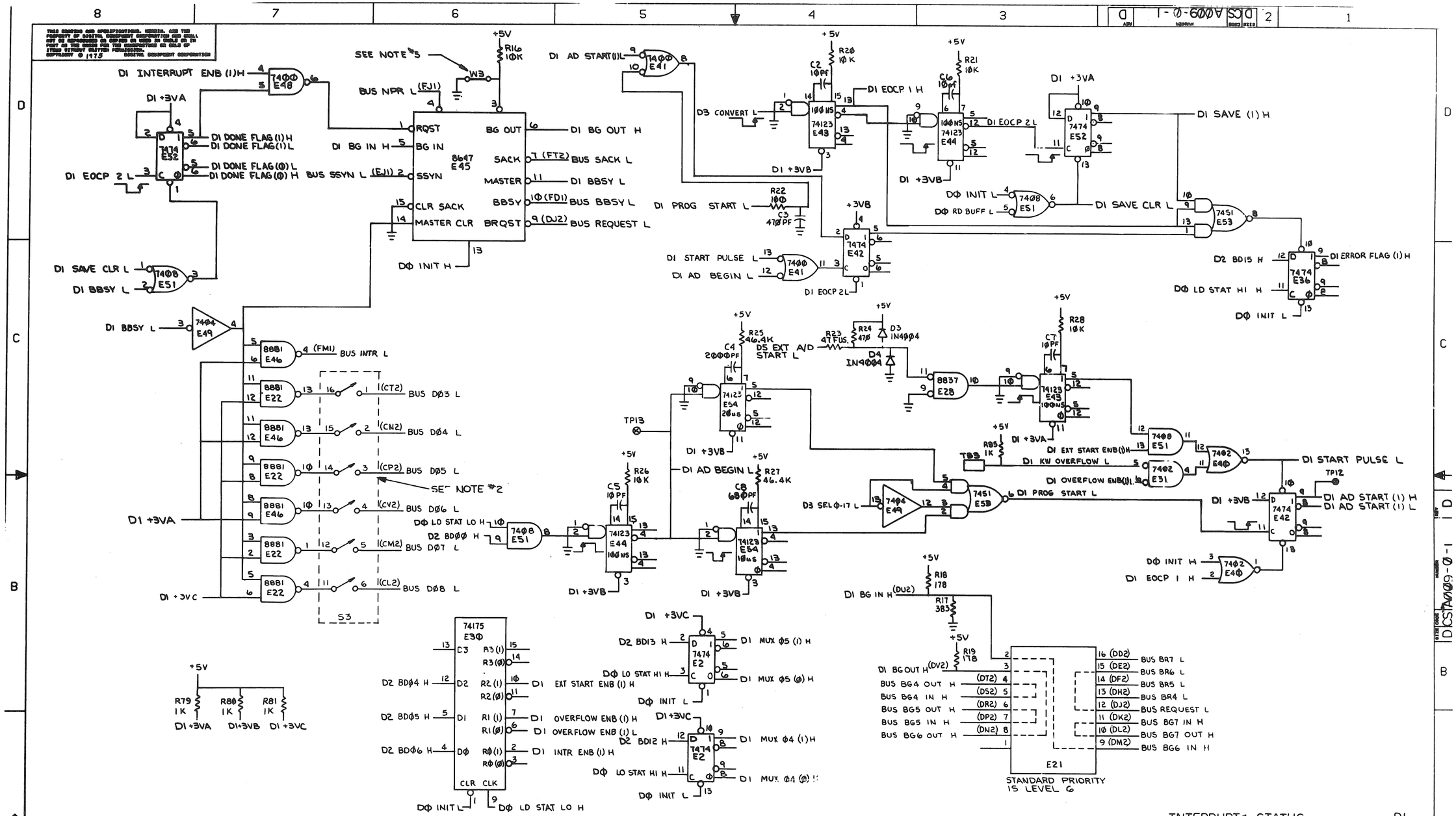
SIGNATURES	DATE
DRN. R.W. Counter	28-OCT-75
CHK'D.	4-Nov-75
ENG	1-9-76
PROJ. ENG	1-9-76
PROD.	

digital

TITLE 12 BIT A/D CONVERTER

SCALE NONE	SIZE D	CODE CS	NUMBER A009-0-1	REV D
SHT. 1 OF 6				
ETCH REV	FIRST USED ON			

MS#



NOTES: 2. VECTOR SWITCH SETTINGS:
OFF FOR A LOGIC "Ø"
ON FOR A LOGIC "1"
5. IN 11/15 OR 11/20 WITHOUT KH11 OPTION, REMOVE W3.

CHR	CHANGE NO	REV

INTERRUPT & STATUS — DI

SIGNATURES	DATE
DRN. M. Quebico	23 Oct 75
CHK'D.	
ENG.	1-9-76
PROJ. ENG.	1-9-76
PROD.	

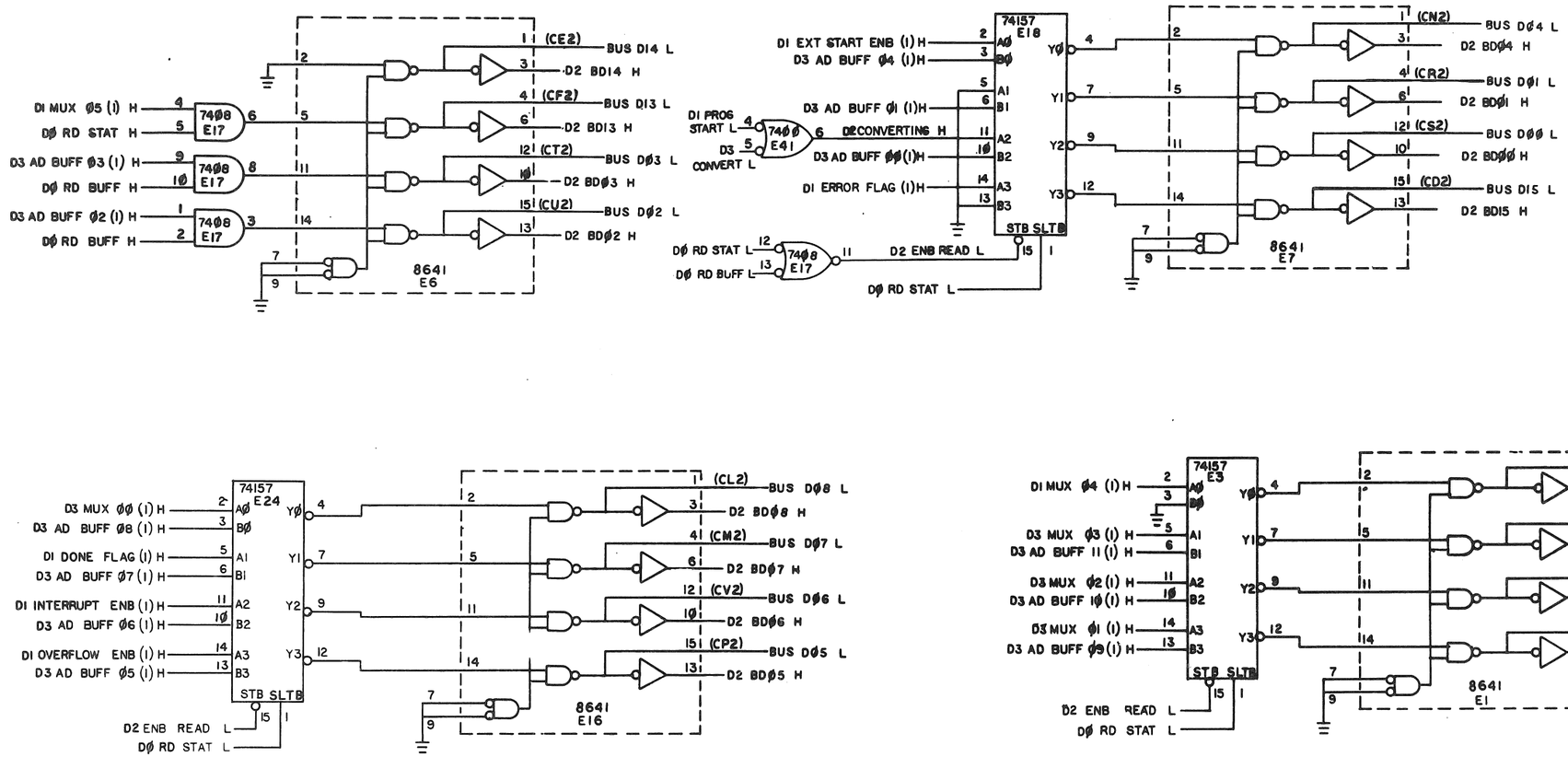
digital

TITLE 12 BIT A/D CONVERTER -

SCALE — SHT. 2 OF 6 — ETCH REV — FIRST USED ON

SIZE	CODE	NUMBER	REV
D	CS	AØØ9-Ø-1	D

1 MS#



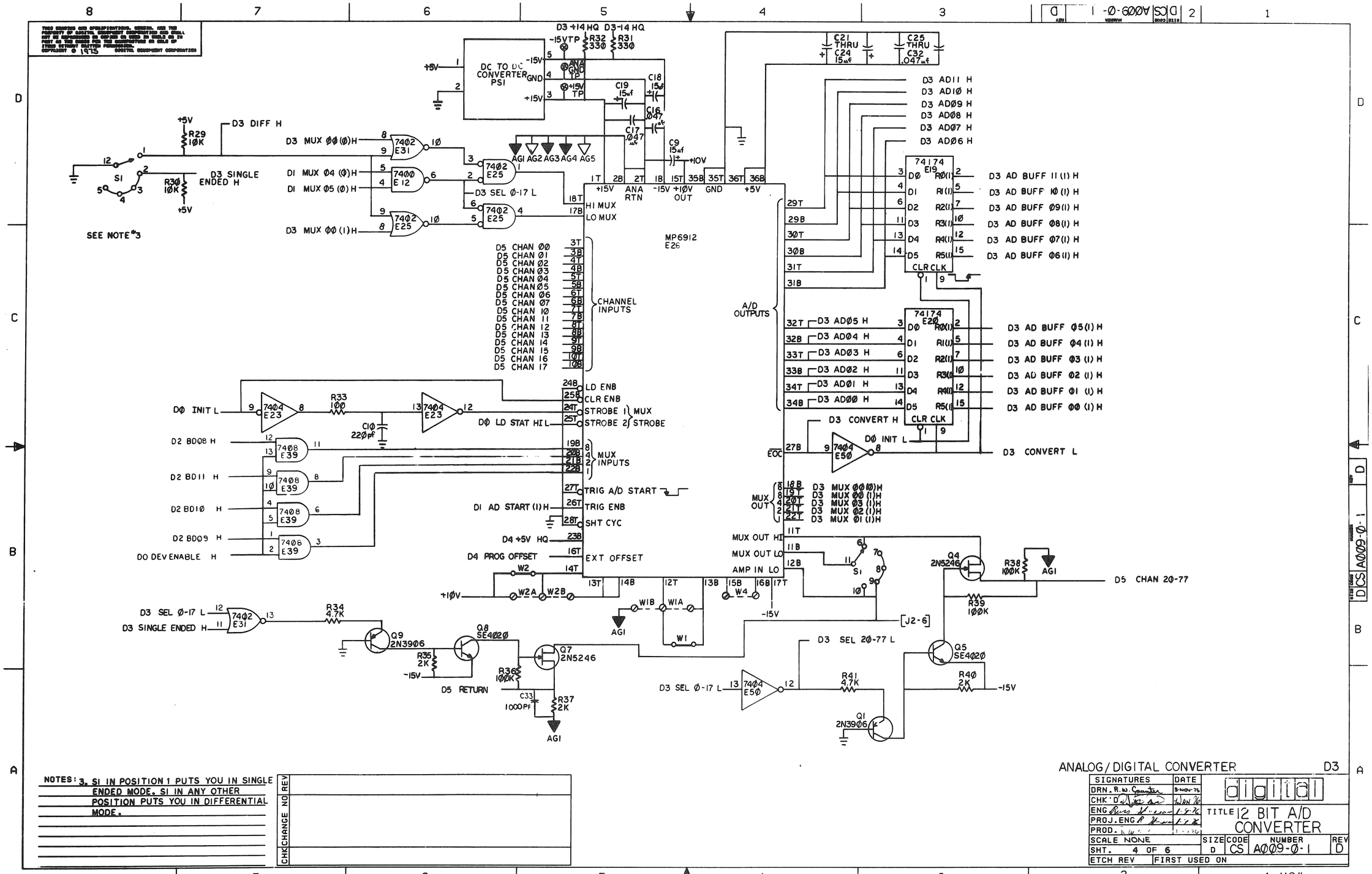
BUS DATA D2

NOTES:

CHK	CHANGE NO	REV

SIGNATURES	DATE	
DRN. M. Quelvie	21 OCT 75	digital
CHK'D.		
ENG.	1-9-76	TITLE 12 BIT A/D CONVERTER
PROJ. ENG.	1-9-76	
PROD.		
SCALE NONE	SIZE D	CODE CS NUMBER AØØ9-Ø-1 REV D
SHT. 3 OF 6		
ETCH REV	FIRST USED ON	

1 MS#



NOTES: 3. S1 IN POSITION 1 PUTS YOU IN SINGLE ENDED MODE. S1 IN ANY OTHER POSITION PUTS YOU IN DIFFERENTIAL MODE.

CHK	CHANGE NO	REV

ANALOG/DIGITAL CONVERTER D3

SIGNATURES	DATE
DRN. R. W. Carpenter	3-NOV-75
CHK'D	
ENG	
PROJ. ENG	
PROD.	

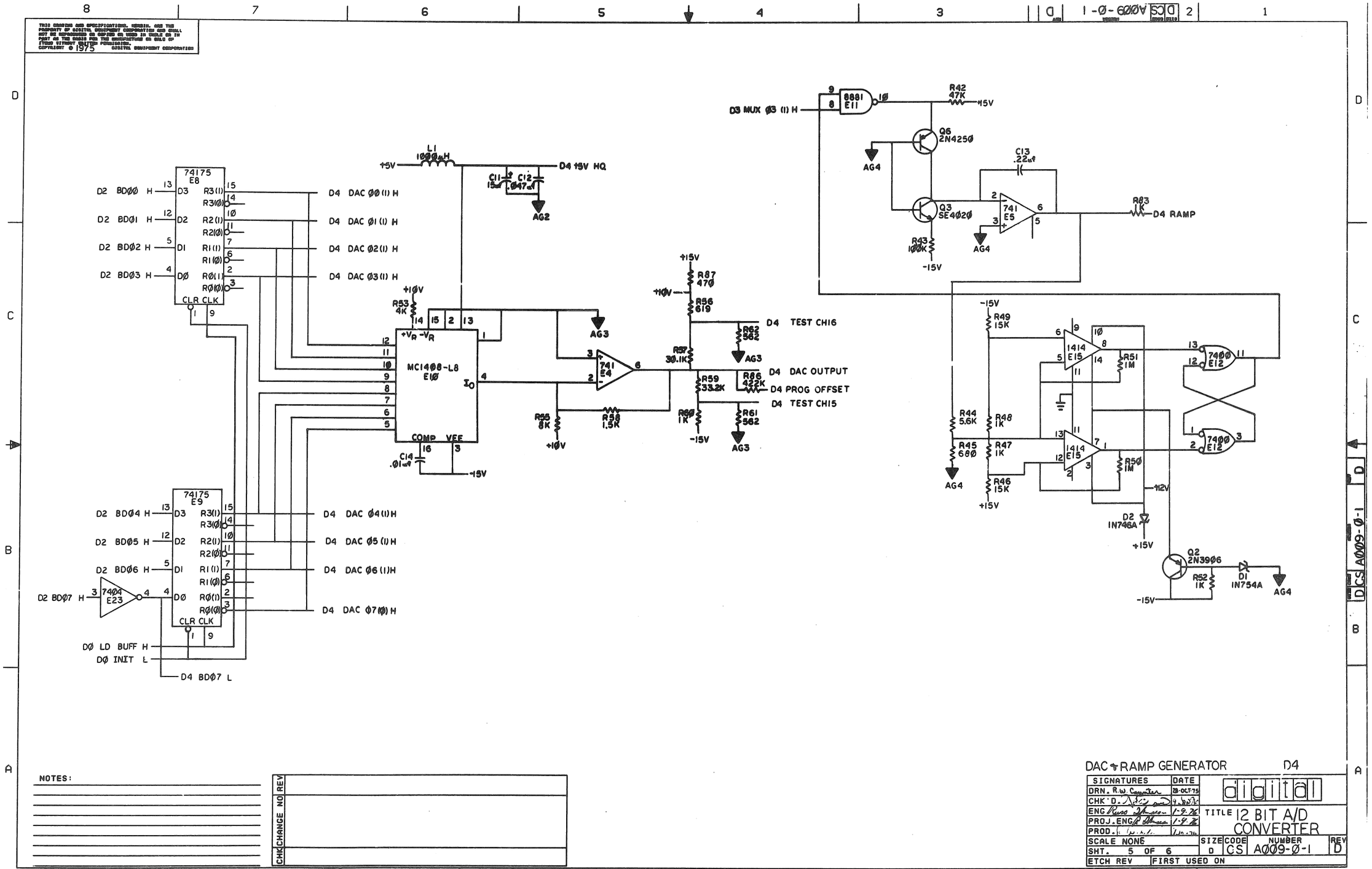
digital

TITLE 12 BIT A/D CONVERTER

SCALE NONE	SIZE	CODE	NUMBER	REV
SHT. 4 OF 6	D	CS	A009-0-1	D

ETCH REV FIRST USED ON

MS#



NOTES:

CHK	CHANGE NO	REV

DAC & RAMP GENERATOR D4

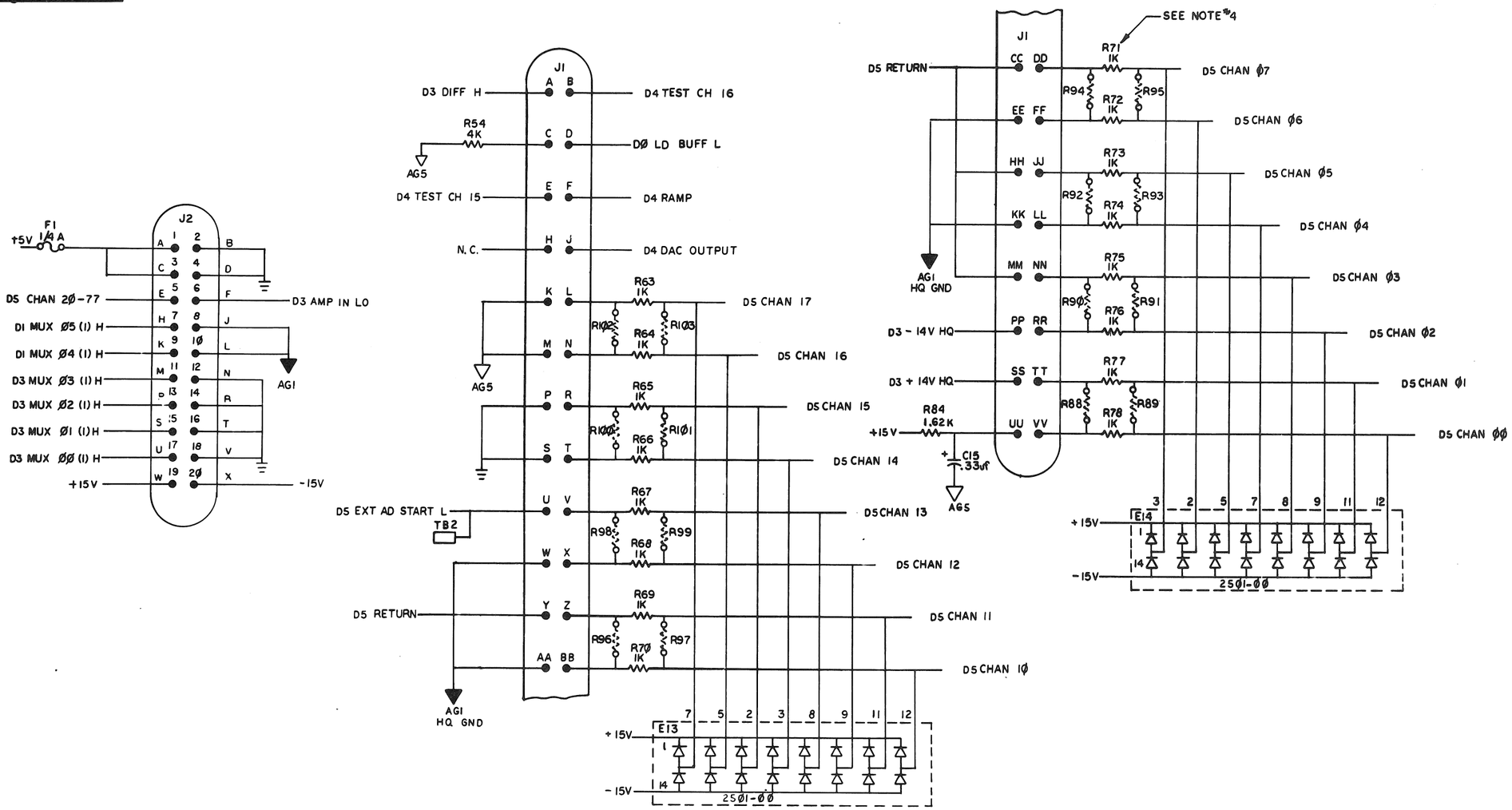
SIGNATURES	DATE
DRN. R.W. Carpenter	28-OCT-75
CHK'D.	
ENG Russ Johnson	1-9-76
PROJ. ENG R. Johnson	1-9-76
PROD.	

digital

TITLE 12 BIT A/D CONVERTER

SCALE NONE	SIZE	CODE	NUMBER	REV
SHT. 5 OF 6	D	CS	A009-Ø-1	D
ETCH REV FIRST USED ON				

MS#



NOTES: 4. ALL 1K RES ON THIS PAGE ARE FUSIBLE.

CHK	CHANGE NO	REV

CABLING

D5

SIGNATURES	DATE
DRN. R.W. Carter	23-OCT-75
CHK'D	
ENG	1-9-76
PROJ. ENG	1-9-76
PROD.	

digital

TITLE 12 BIT A/D CONVERTER

SCALE NONE	SIZE	CODE	NUMBER	REV
SHT. 6 OF 6	D	CS	AØØ9-Ø-1	D
ETCH REV FIRST USED ON				

MS#

NOTES:

1. FOR DRAWING DIRECTORY, REFER TO: B-DO-A009-0
2. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE TYPE	VCC	GND
16 PIN DIP	16	8
14 PIN DIP	14	7
I.C. DEC 741	7	1

3. SPARE LOCATIONS ARE: R00 THRU R103,E47

REWORK INSTRUCTIONS

ETCH CUTS SIDE 1 (AS SHOWN)

1. CUT ETCH ON RUN FROM PTH TO THE RIGHT OF E25
2. CUT ETCH AT PTH ABOVE AND TO THE RIGHT OF Q4

ETCH CUTS SIDE 2 (AS SHOWN)

1. CUT ETCH AT S1(6)
2. CUT ETCH TO THE RIGHT OF S1(4)

WIRE ADDS SIDE 1 (AS SHOWN)

1. DRILL HOLE TO DIMENSION SHOWN. ADD WIRE FROM PTH BELOW R43 THRU DRILL HOLE TO S1(6) ON SIDE 2.
2. ADD WIRE FROM PTH TO THE LEFT OF S1(4) TO E26(11B) (AT ETCH JUST UNDER E26(23T).

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
2	E4,E6	I.C. DEC 741	1910200	53
3	E8,E9,E30	I.C. DEC 74175	1910651	54
1	E10	I.C. DEC MC1400	1911020	55
3	E11,E22,E40	I.C. DEC 8001	1908705	56
3	E12,E41,E48	I.C. DEC 7400	1905575	57
2	E13,E14	I.C. DEC 2501 DIODE PACK	1910010-00	58
1	E15	I.C. DEC MC1414L	1910337	59
3	E17,E39,E51	I.C. DEC 7408	1910155	60
2	E19,E20	I.C. DEC 74174	1910652	61
1	E21	PRIORITY SOCKET	1209830	62
3	E23,E49,E50	I.C. DEC 7404	1909866	63
3	E25,E31,E40	I.C. DEC 7402	1908004	64
1	E27	I.C. DEC 8640	1911469	65
3	E28,E32,E33	I.C. DEC 8637	1911118	66
3	E29,E37,E38	I.C. DEC 8242	1909712	67
1	E34	I.C. DEC 7410	1905576	68
1	E35	I.C. DEC 74155	1910656	69
3	E43,E44,E54	I.C. DEC 74123	1910436	70
1	E45	I.C. DEC 8647	1912083	71
1	E53	I.C. DEC 7451	1905628	72
1	XE21	PRIORITY JUMPER LEVEL #6	5400780	73
1	J1	CONN. 40 PIN	1209941-02	74
1	J2	CONN. RT ANGLE HEADER 20 PIN	1209941-06	75
1	J3	CONN. 72 PIN	1213065	76
1	S1	SWITCH 2P 5POS	1209808	77
1	S2	SWITCH PACK (10)	1211164-08	78
1	S3	SWITCH PACK (8)	1211164-04	79
1	F1	FUSE ¼A PICO	1210829-04	80
3	W1,W2,W3	JUMPER, WHT INSULATION	9009185	81
1		LATCH, L.H.	1209941-03	82
1		LATCH, R.H.	1209941-04	83
13		SPLIT LUG	9008735	84
2		HANDLE, FLIP CHIP (ORANGE)	9009337-00	85
4		EYELETS	9008732	86
2		FASTONS	9007112	87
2		EYELETS	9008000	88

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1		ETCHED CIRCUIT BOARD	5011858	1
2	C1,C5	CAP. 470pf 100V 5%	1000024	2
4	C2,C6,C8,C7	CAP. 10pf 100V 5%	1000006	3
1	C4	CAP. 2000pf 500V 5%	1002315	4
1	C8	CAP. 680pf 100V 5%	1000026	5
8	C9,C11,C18,C19,C21 THRU C24	CAP. 15mf 20V 10%	1004812	6
1	C10	CAP. 220pf 100V 5%	1000021	7
11	C12,C16,C17,C25 THRU C32	CAP. .047µf 50V	1012784	8
1	C13	CAP. .22mf 50V 10%	1010031-03	9
1	C14	CAP. .01mf 100V 20%	1001610-01	10
1	C15	CAP. .33mf 20V 10%	1005328	11
1	C33	CAP. 1000pf 100V 5%	1000042	12
1	D1	DIODE 1N754A	1109991-00	13
1	D2	DIODE 1N746A	1104880	14
2	D3,D4	DIODE 1N4004	1105796	15
19	R1 THRU R12,R16,R20,R21, R26,R28,R29,R30	RES. 10K 5% ¼W	1300479	16
10	R13,R14,R47,R48,R52,R79, R80,R81,R83,R85	RES. 1K 5% ¼W	1300365	17
3	R15,R22,R33	RES. 100 5% ¼W	1300220	18
1	R17	RES. 383 1% ¼W	1305125	19
2	R18,R19	RES. 178 1% ¼W	1311422	20
1	R23	RES. 47 1% ¼W	1310861-02	21
2	R24,R87	RES. 470 5% ¼W	1300318	22
2	R25,R27	RES. 40.4K 1% ¼W	1303311	23
2	R31,R32	RES. 330 5% ¼W	1300295	24
2	R34,R41	RES. 4.7K 5% ¼W	1300447	25
3	R35,R37,R40	RES. 2K 5% ¼W	1302398	26
4	R36,R38,R39,R43	RES. 100K 5% ¼W	1302466	27
1	R42	RES. 47K 5% ¼W	1302177	28
1	R44	RES. 5.6K 5% ¼W	1301874	29
1	R45	RES. 680 5% ¼W	1301424	30
2	R46,R49	RES. 15K 5% ¼W	1300498	31
2	R50,R51	RES. 1M 5% ¼W	1309595	32
2	R53,R54	RES. 4K 1% ¼W	1305127	33
1	R55	RES. 8K 1% ¼W	1305129	34
1	R56	RES. 619 1% ¼W	1305126	35
1	R57	RES. 30.1K 1% ¼W	1311594	36
1	R58	RES. 1.5K 1% ¼W RN55C-F	1301980	37
1	R59	RES. 33.2K 1% ¼W	1305420	38
1	R60	RES. 1K 1% ¼W	1302748	39
2	R61,R62	RES. 562 1% ¼W	1304693	40
18	R63 THRU R78	RES. 1K 1% ¼W FUSIBLE	1310881-00	41
1	R84	RES. 1.62K 1% ¼W	1304962	42
1	R86	RES. 422K 1% 1/8W RN55C-F	1310607	43
3	Q1,Q2,Q9	TRANS. 2N3906	1509525	44
3	Q3,Q5,Q8	TRANS. SE4020	1509567	45
2	Q4,Q7	TRANS. 2N5246	1512721	46
1	Q6	TRANS.DEC4250	1509142	47
1	L1	INDUCTOR 1000uH 5%	1602723	48
1	PS1	CONVERTER DC-DC PS2402	1911207	49
4	E1,E6,E7,E16	I.C. DEC 8641	1911579	50
4	E2,E36,E42,E52	I.C. DEC 7474	1905547	51
3	E3,E18,E24	I.C. DEC 74157	1910855	52

PARTS LIST

FIRST USED ON O/P: ADII-K

ETCH BOARD REV

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO.	REVISIONS	CHK	ORIGINATED
E	A009-00004		P.TURCOTTE 28-SEPT-76	P.TURCOTTE 27-SEPT-76

DRN. R. Samaché 16/JULY/76
CHK'D. R.W. Cantin 20 AUG 76
ENG. P. Turcotte 27-SEPT-76
FIELD ENG. P. Turcotte 27-SEPT-76
PROD. 13-SEPT-76
NEXT HIGHER ASSY B-DD-A009-0
SCALE
SHEET 1 OF 4

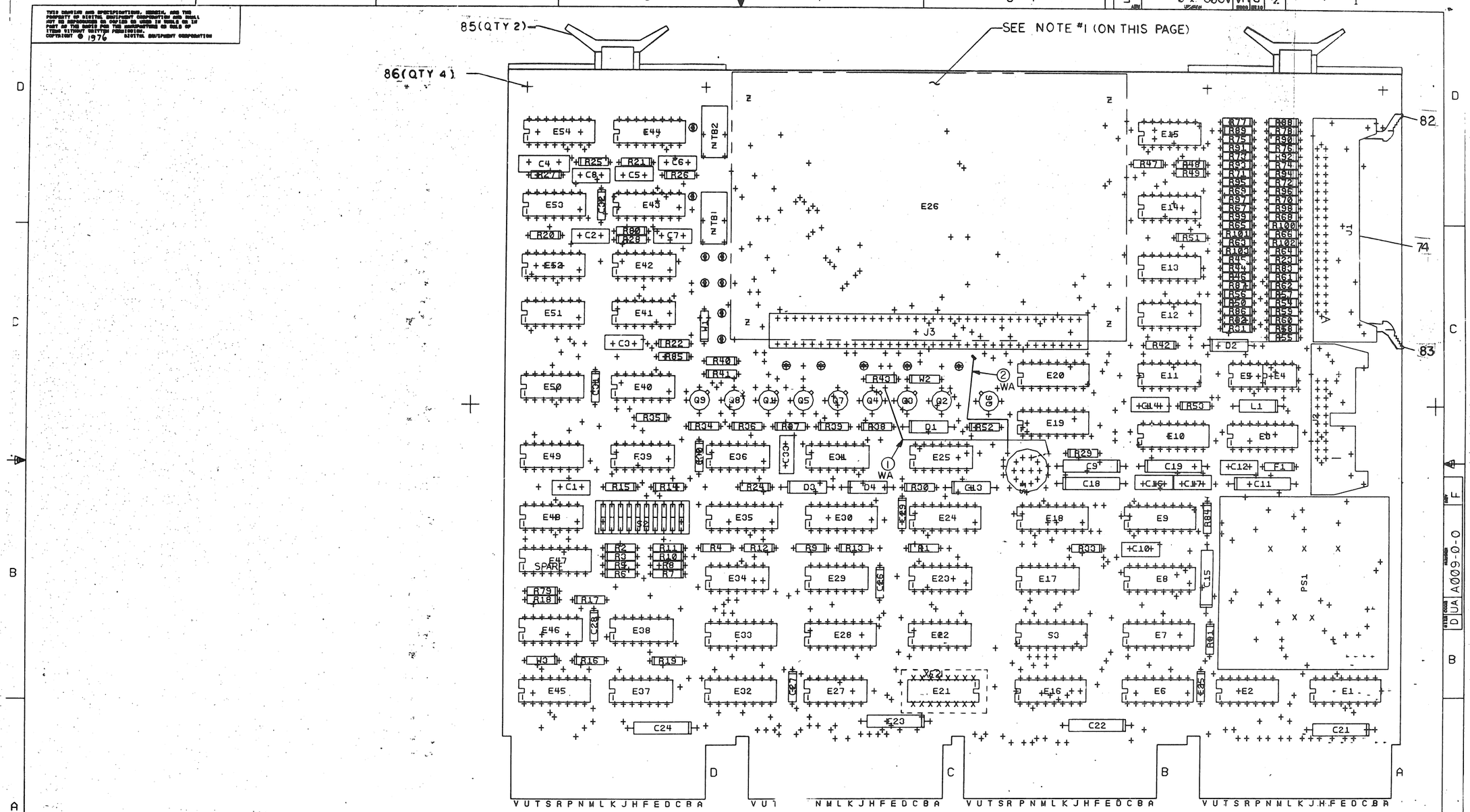
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE 12 BIT A/D CONVERTER

SIZE	CODE	NUMBER	REV.
D	UA	A009-0-0	F

DIST.

DEC FORM NO DRD-135



NOTES: 1. A/D CONVERTER PACKAGE AND HARDWARE SHOULD BE PICKED UP AT A HIGHER ASSY. SEE D-UA-ADII-K-Ø

CHK	CHANGE NO	REV

SIGNATURES	DATE
DRN. Paul Lucian	28 JUL 76
CHK'D. R W Conover	21 AUG 76
ENG. Cat Smyth	9 SEP 76
PROJ. ENG. Cat Smyth	9 SEP 76
PROD. Al Wakefield	13 SEP 76

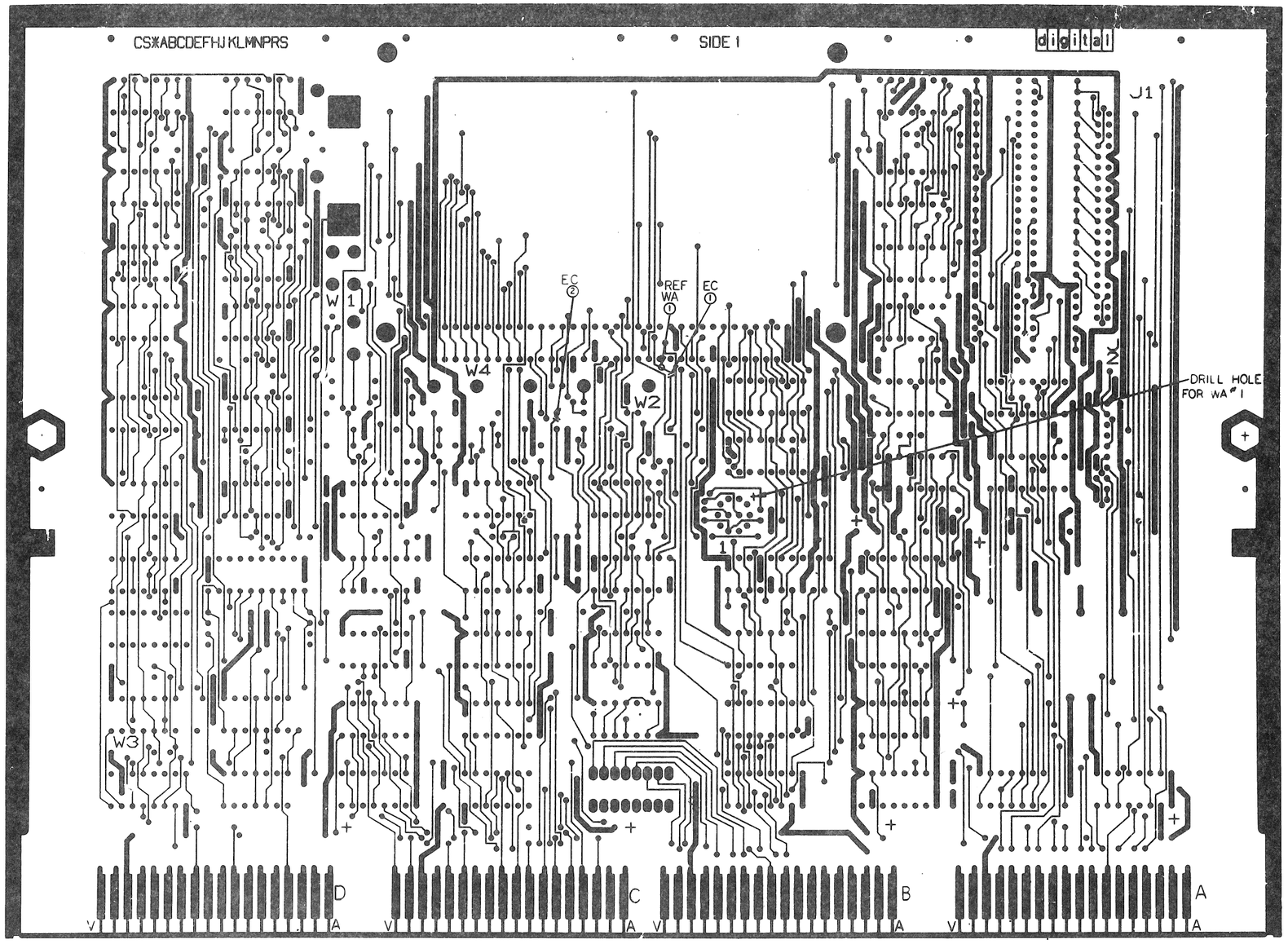
digital

TITLE 12 BIT A/D CONVERTER

SCALE 2/1	SIZE	CODE	NUMBER	REV
SHT. 2 OF 4	D	UA	A009-0-0	F

NEXT HIGHER ASSY. B-DD-A009-0

MS# 30333



NOTES:

CHK	CHANGE NO	REV

SIGNATURES	DATE
DRN.	21 JULY 76
CHK'D.	
ENG.	9-SEP-76
PROJ. ENG.	9-SEP-76
PROD.	13 SEP 76

digital

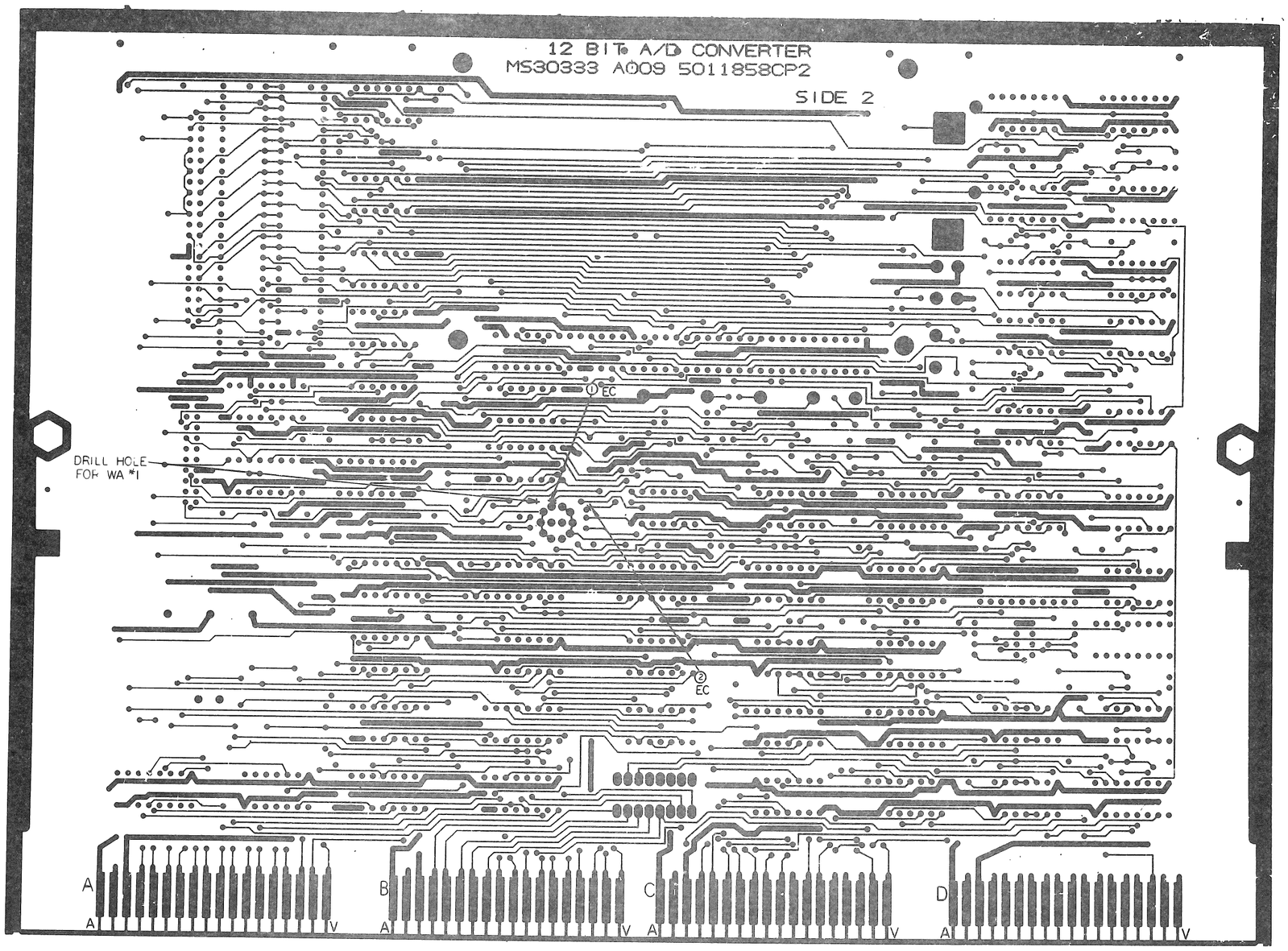
TITLE 12 BIT A/D CONVERTER

SCALE	SIZE	CODE	NUMBER	REV
2/1	D	UA	A009-0-0	F

SHT. 3 OF 4

ETCH REV C | FIRST USED ON ADII-K

MS# 30333



NOTES:

CHK	CHANGE NO	REV

SIGNATURES	DATE
DRN.	21 JUL 76
CHK'D.	
ENG	7-SEP-76
PROJ. ENG	7-SEP-76
PROD.	13-SEP-76

digital

TITLE 12 BIT A/D CONVERTER

SCALE 2/1	SIZE	CODE	NUMBER	REV
SHT. 4 OF 4	D	UA	A009-0-0	F
ETCH REV C	FIRST USED ON ADII-K			

1 MS# 30333

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

	SEQUENCE
12 BIT A/D CONVERTER	D-UA-AØØ9-Ø-Ø
12 BIT A/D CONVERTER	D-CS-AØØ9-Ø-1

SEQUENCE

THIS IS PRINT SET

UNIT VARIATIONS		PRINT SET
VAR	TITLE	
AØØ9	12 BIT A/D CONVERTER	

REVISIONS			
DATE	CHG. NO.	REV
RBJ	00001	A
RBJ	00002	B
RBJ	00003	C
P.L.	00004	D
1-77	00005	E

USED ON OPTION/MODEL	
AD11-K	

DRN. R.W. Carrier	DATE 19-DEC-75	TITLE	
CHK'D.	DATE 16 JAN '76	12 BIT A/D CONVERTER	
PROJ ENG. Russ Ohnsian	DATE 1-9-76		
PROD.	DATE 7 JAN 76	SIZE B	CODE DD	NUMBER AØØ9-Ø	REV E
FIELD SERV.	DATE 9 JAN '76	DIST	

SHEET 1 OF 2

EN-01062-1A-16-R972-(325)

DRB 106

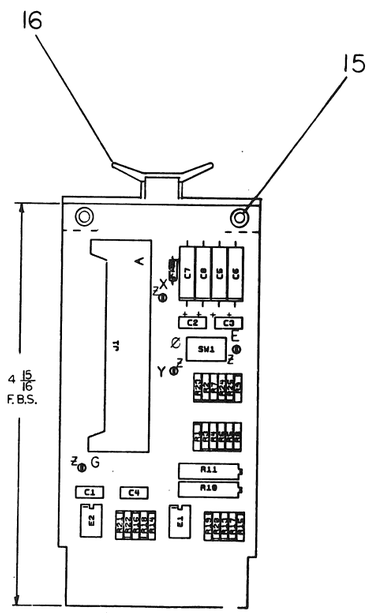
REVISION CONTROL SHEET

CUSTOMER PRINT SET	MFG SET	DRAWING NO	NO OF SHT	DESCRIPTION	OPTION NO/FILE DATE	REVISIONS					
		D-UA-AØØ9-Ø-Ø	4	12 BIT A/D CONVERTER		A	B	C	D	E	F
		D-CS-AØØ9-Ø-1	6	12 BIT A/D CONVERTER		A	B	C	C	D	D
		K-CO-AØØ9-Ø-4	1	12 BIT A/D CONVERTER (CALDEC DATA BASE)		B	B	B	B	C	C
		D-AH-AØØ9-Ø-5	2	12 BIT A/D CONVERTER		A	B	B	B	C	D
		B-MH-AØØ9-Ø-6	1	MODULE ECO HISTORY		REF	-	-	-	-	-
		5011858	-	ETCH CIRCUIT BOARD		B	B	B	B	C	C
		ECO NO				ORIG	00001	00002	00003	00004	00005

CUSTOMER PRINT SET CODES
X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE		SIZE	CODE	NUMBER	REV
	A/D CONVERTER SHEET 2 OF 2	B	DD	AØØ9-Ø	E

NOTES:



REF		DESCRIPTION	PART NO	ITEM NO
REF		X-Y COORDINATE HOLE LOCATION	K-CO-G5036-0-4	1
REF		ASSY DRILLING HOLE LAYOUT	G-AH-G5036-0-5	2
REF		MODULE ECO HISTORY	B-MH-G5036-0-6	3
1		ETCH CIRCUIT BOARD	5011045	4
4	C1 THRU C4	CAP. .01 µf. 100V. 20% DISC	1001610-01	5
4	C5 THRU C8	CAP. 15 µf. 20V. 10% TANT	1004812	6
1	J1	CONN. 40 PIN	1209941	7
5	R1, R13 THRU R16	RES. 100K 1/4W 1% (RN55D-1003F)	1303044	8
5	R2, R8, R23, R24, R25	RES. 4K 1/4W 1% (RN55D-4001F)	1305127	9
5	R3, R9, R17, R18, R26	RES. 1K 1/4W 1% (RN55D-1001F)	1303114	10
2	R4, R7	RES. 9.09K 1/4W 1% (RN55D-9091F)	1304855	11
6	R5, R6, R19 THRU R22	RES. 1.992K 1/4W 1% (RN55E-1992B)	1302677	12
2	R10, R11	RES. 10K POT 3/4W 10% TC PR	1309143-10	13
2	E1, E2	IC DEC 741	1910298	14
2		EYELET	9006732	15
1		HANDLE, FLIP CHIP GREEN	9008337-01	16
1	SW1	SWITCH SPDT	1209698	17
4		SPLIT LUGS	9006735	18

QTY | REF DESIGNATION | DESCRIPTION | PART NO | ITEM NO

PARTS LIST

ETCH BOARD REV B

FIRST USED ON OPTION MODEL

IC TYPE	GND	+ 5V	-VCC	+VCC
DEC 741	-	-	4	7

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO.	CHK
B	65036-00001	

REVISIONS

A. BILZ 5-14-75

DRN. 1/9/74 · CHK'D. 7/17/74 · ENG. 7/24/74 · PROJ. ENG. 7/24/74 · PROD. 7/24/74

NEXT HIGHER ASSY

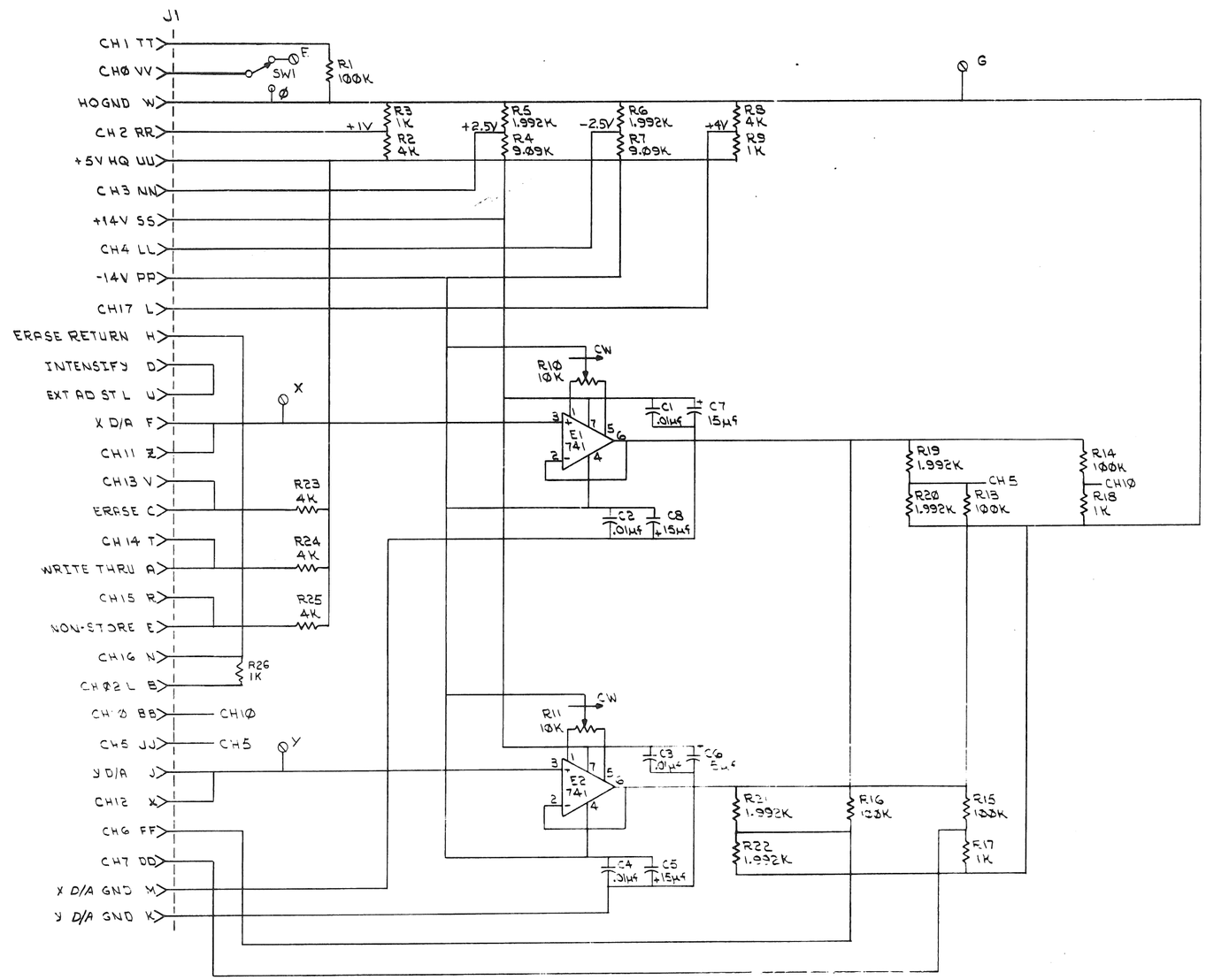
SCALE NONE · SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE WRAP AROUND

SIZE D · CODE CS · NUMBER G5036-0-1 · REV. B · DIST.

D CS G5036-0-1 B



REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
WRAP AROUND	D	CS	G5Ø36-Ø-1	B
SCALE NONE	SHEET 2 OF 2	DIST.		

DEC FORM NO
DEC 120