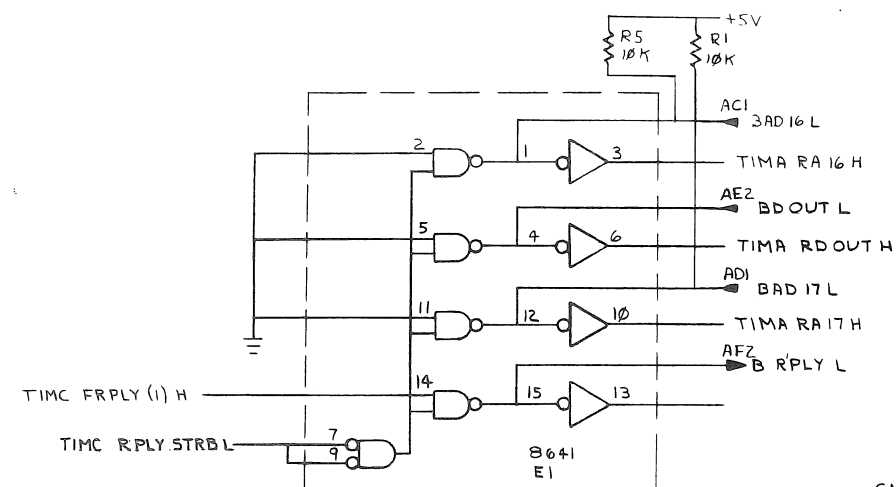
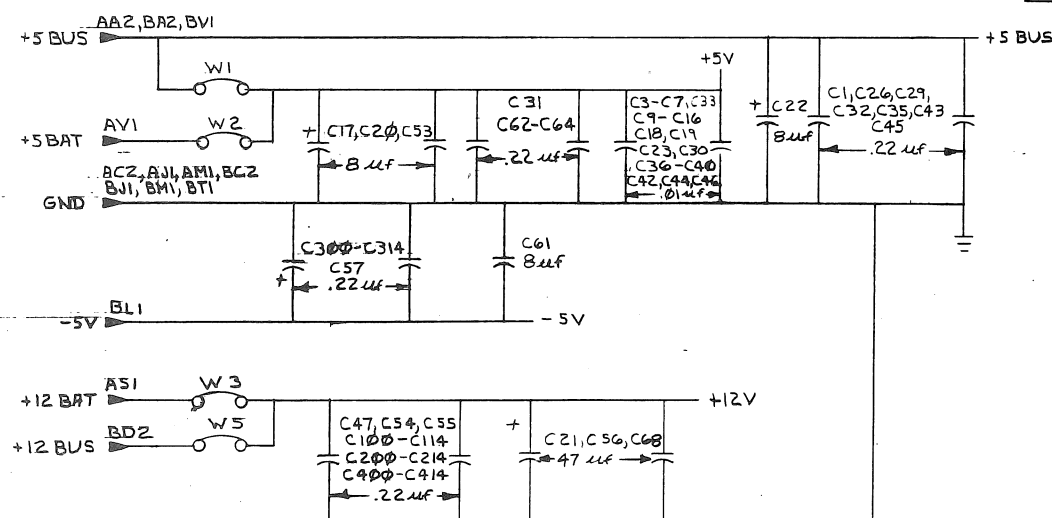


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BUS INTERFACE LOGIC

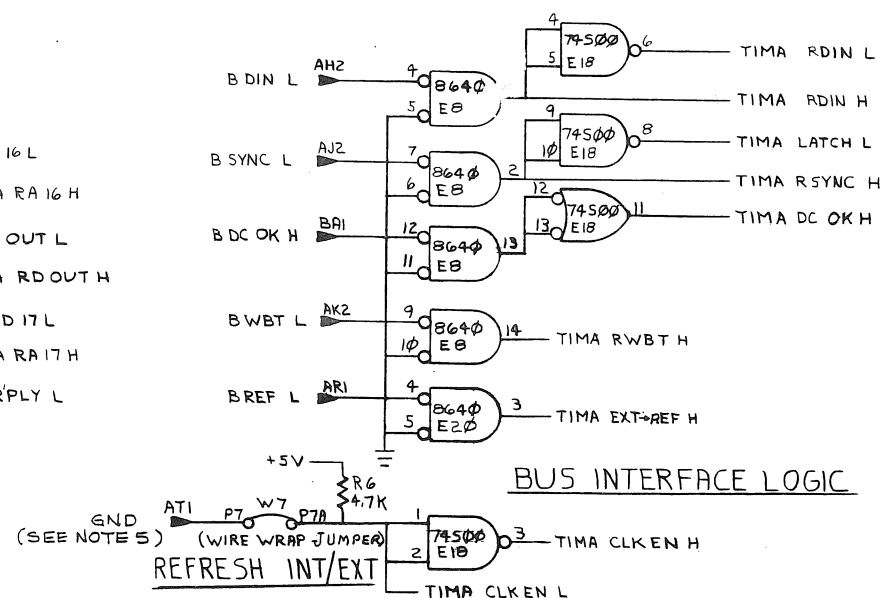


NOTES:

- OPTION DESIGNATION:
M7955-AA=M7955-YA OR M7955-YE
M7955-AB=M7955-YB OR M7955-YF
M7955-AC=M7955-YC OR M7955-YH
M7955-AD=M7955-YD OR M7955-YJ
- ALL 8641 BUS REC/DR PLUS 7483A ADDER AND 745138 DECODER ARE POWERED BY +5V BUS. ALL OTHER CIRCUITS GO TO +5V AS SELECTED BY W1 & W2.
- W1, W2, W3, W5, W14, W15 ARE MACHINE INSERTABLE JUMPERS. W4, W6, W7, W8, W12, W16 ARE WIRE WRAP JUMPERS.
- ALL BDAL-XX CONNECTIONS ARE BI-DIRECTIONAL LINES
- DURING MANUFACTURING TEST, GROUND MAY BE REMOVED

NOT USED REF DES

C100-C114, C200-C214, W8, W12, W16
C100-C114, C200-C214, W12, W16
C100-C114, W16



BUS INTERFACE LOGIC

REFRESH INT/EXT

AR2 AS2

AM2 AN2

CM2 W14 CN2

CR2 W15 CS2

BUS GRANT CONTINUITY JUMPERS

W6 W7 REFRESH OPTIONS

IN	IN	INTERNAL REFRESH WITH NO B R'PLY
IN	OUT	EXTERNAL REFRESH WITH NO B R'PLY
OUT	IN	ILLEGAL
OUT	OUT	EXTERNAL REFRESH WITH B R'PLY

REFRESH SELECTION

M7955 VARIATIONS JUMPERS -AA -AB -AC -AD

JUMPERS	-AA	-AB	-AC	-AD
W4	1	1	1	1
W8	0	1	1	1
W12	0	0	1	1
W16	0	0	0	1

ALL JUMPERS NOTED AS 0 MUST NOT BE INSTALLED

STARTING ADDRESS	SWITCH S1 SETTINGS
0	1 1 1 1 1
4K	0 1 1 1 1
8K	1 0 1 1 1
12K	0 0 1 1 1
16K	1 1 0 1 1
20K	0 1 0 1 1
24K	1 0 0 1 1
28K	0 0 0 1 1
32K	1 1 1 0 1
36K	0 1 1 0 1
40K	1 0 1 0 1
44K	0 0 1 0 1
48K	1 1 0 0 1
52K	0 1 0 0 1
56K	1 0 0 0 1
60K	0 0 0 0 1
64K	1 1 1 1 0
68K	0 1 1 1 0
72K	1 0 1 1 0
76K	0 0 1 1 0
80K	1 1 0 1 0
84K	0 1 0 1 0
88K	1 0 0 1 0
92K	0 0 0 1 0
96K	1 1 1 0 0
100K	0 1 1 0 0
104K	1 0 1 0 0
108K	0 0 1 0 0
112K	1 1 0 0 0
116K	0 1 0 0 0
120K	1 0 0 0 0
124K	0 0 0 0 0

STARTING ADDRESS SELECTION

EXCEPT M7955-AD
EXCEPT M7955-AC & AD
EXCEPT M7955-AB, AC, & AD

OVER LAPPING IS NOT ALLOWED IN ANY PERIPHERAL PAGE

IC PIN LOCATIONS

I.C. TYPE	GND	+5	+12
555 @ E2	1	8	
555 @ E44	1		8
7493	10	5	
7483A	12	5	
74LS75	12	5	
8640	1	8	
OTHER 16 PIN I.C.'S	8	16	
OTHER 14 PIN I.C.'S	7	14	

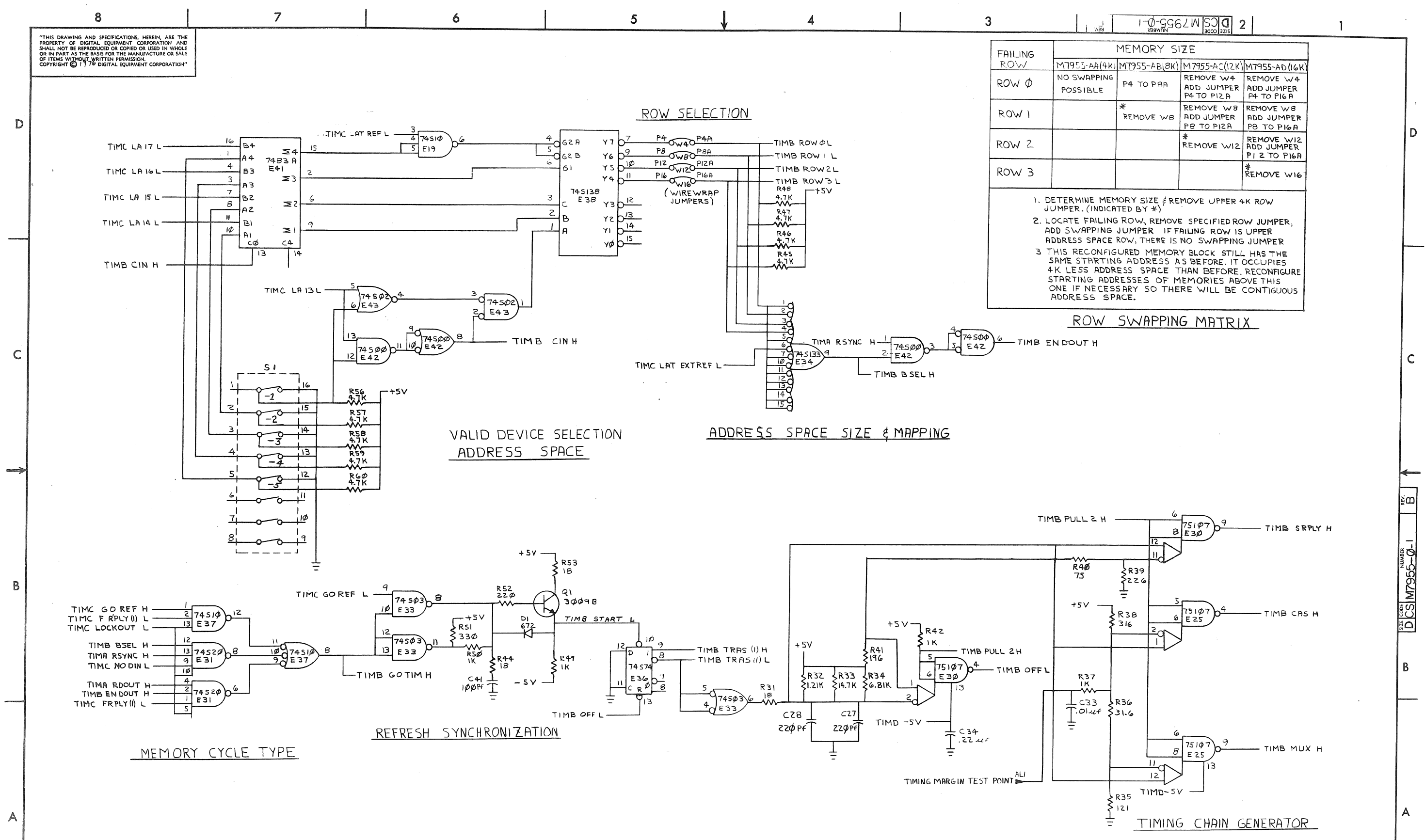
DRN. Rev. 1.0 11/10/76	FIRST USED ON MSV11-C	DIGITAL
CHK'D. J. R. 11/10/76	TITLE MSV11-C MOS MEMORY, LSI (TIMA)	
ENG. J. R. 11/10/76		
PROJ. ENG. J. R. 11/10/76		
PROD. R. 11/10/76		
NEXT HIGHER ASSY.		
B-DD-M7955-0-0	SIZE CODE NUMBER	REV. B
SCALE	D CS M7955-0-1	
SHEET 1 OF 8	DIST.	

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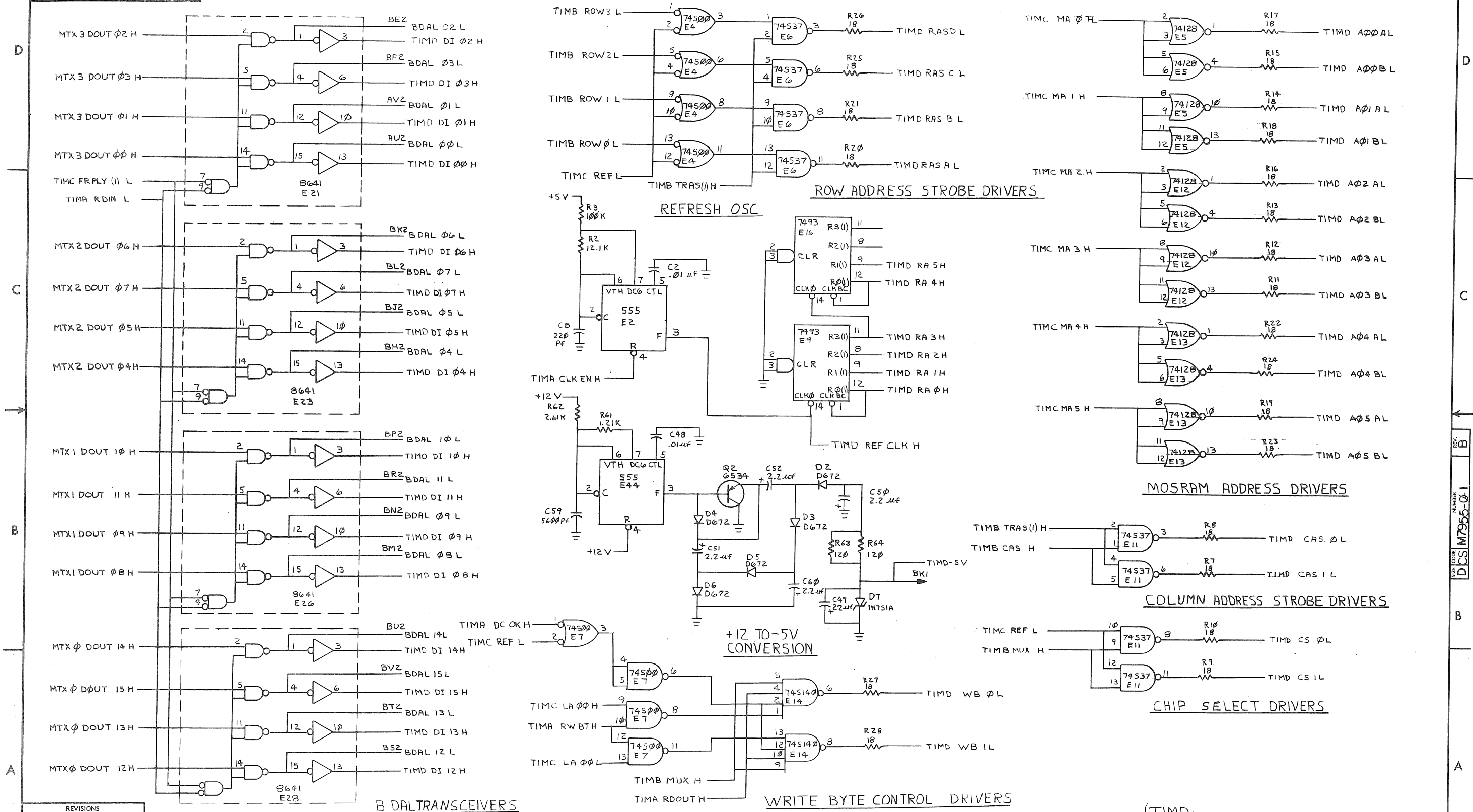
FAILING ROW	MEMORY SIZE			
	M7955-AA(4K)	M7955-AB(8K)	M7955-AC(12K)	M7955-AD(16K)
ROW 0	NO SWAPPING POSSIBLE	P4 TO P8A	REMOVE W4 ADD JUMPER P4 TO P12A	REMOVE W4 ADD JUMPER P4 TO P16A
ROW 1		* REMOVE W8	REMOVE W8 ADD JUMPER P8 TO P12A	REMOVE W8 ADD JUMPER P8 TO P16A
ROW 2			* REMOVE W12	REMOVE W12 ADD JUMPER P12 TO P16A
ROW 3				* REMOVE W16

1. DETERMINE MEMORY SIZE & REMOVE UPPER 4K ROW JUMPER. (INDICATED BY *)
2. LOCATE FAILING ROW, REMOVE SPECIFIED ROW JUMPER, ADD SWAPPING JUMPER IF FAILING ROW IS UPPER ADDRESS SPACE ROW, THERE IS NO SWAPPING JUMPER
3. THIS RECONFIGURED MEMORY BLOCK STILL HAS THE SAME STARTING ADDRESS AS BEFORE. IT OCCUPIES 4K LESS ADDRESS SPACE THAN BEFORE. RECONFIGURE STARTING ADDRESSES OF MEMORIES ABOVE THIS ONE IF NECESSARY SO THERE WILL BE CONTIGUOUS ADDRESS SPACE.

ROW SWAPPING MATRIX



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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		(TMD)	SIZE CODE	NUMBER	REV.
MSV11-C MOS MEMORY LSI		D CS	M7955-0-1	B	
SCALE		SHEET 4 OF 8	DIST.		

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1-0-9962W500 2

D
C
B
A

D
C
B
A

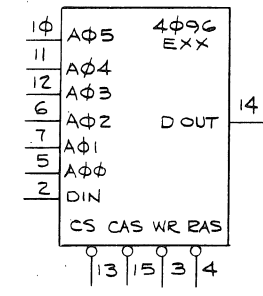
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TIMD A04BL
TIMD A03BL
TIMD A02BL
TIMD A01BL
TIMD A00BL

TIMD DI15H
TIMD CS0L
TIMD CAS0L
TIMD WB0L
TIMD RAS0L

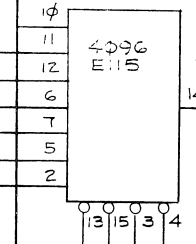
TIMD RASC L
TIMD A05AL
TIMD A04AL
TIMD A03AL
TIMD A02AL
TIMD A01AL
TIMD A00AL

TIMD CS1L
TIMD CAS1L
TIMD RAS1L

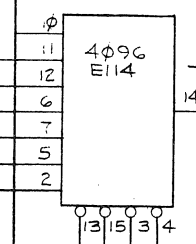
TIMD RASAL



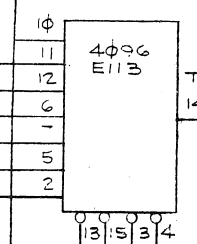
GND PIN 16
5V PIN 1
+12V PIN 8
+5V PIN 9



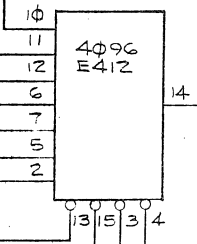
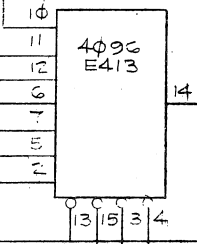
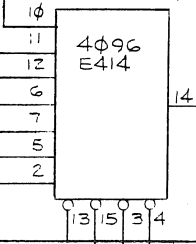
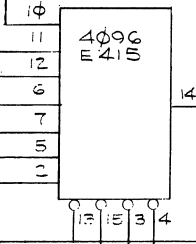
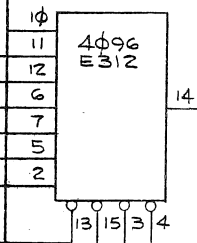
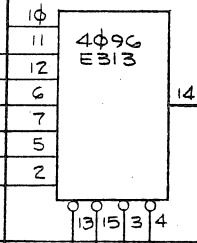
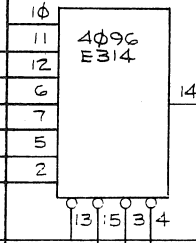
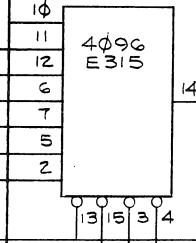
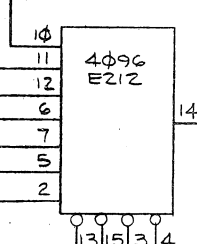
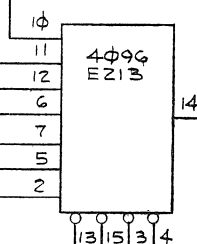
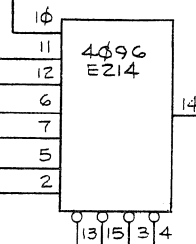
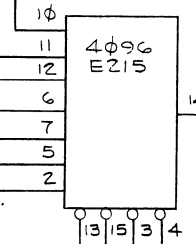
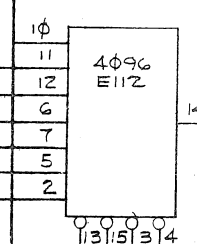
TIMD DI14H



TIMD DI13H



TIMD DI12H



MTX0 15 H

MTX0 14 H

MTX0 13 H

MTX0 12 H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
MSV11-C MOS MEMORY, LSI		D CS	M7955-0-1	B
SCALE	SHEET	OF	DIST.	
	5	8		

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TIMD A05 BL
TIMD A04 BL
TIMD A03 BL
TIMD A02 BL
TIMD A01 BL
TIMD A00 BL

TIMD DI11 H

TIMD CS0 L

TIMD CAS0 L

TIMD WB1 L

TIMD RAS D L

TIMD RAS C L

TIMD A05 AL

TIMD A04 AL

TIMD A03 AL

TIMD A02 AL

TIMD A01 AL

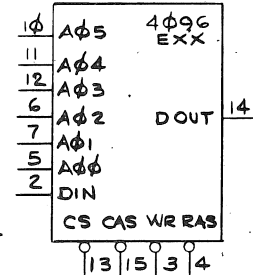
TIMD A00 AL

TIMD CS1 L

TIMD CAS1 L

TIMD RAS B L

TIMD RAS A L



GND PIN 16
-5V PIN 1
+12V PIN 8
+5V PIN 9

MTX111 H

MTX110 H

MTX009 H

MTX008 H

(ARRAY) DATA BITS (11-8) MTX1

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
MSVII-CMOS MEMORY, LSI		D CS	M7955-0-1	B
SCALE		SHEET	OF	DIST.
11		6	8	

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TIMD Aφ5 BL
TIMD Aφ4 BL
TIMD Aφ3 BL
TIMD Aφ2 BL
TIMD Aφ1 BL
TIMD Aφφ BL

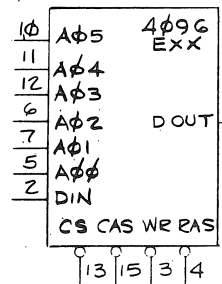
TIMD DI φ7H

TIMD CS φ L
TIMD CAS φ L
TIMD WB φ L
TIMD RAS DL

TIMD RAS CL
TIMD Aφ5 AL
TIMD Aφ4 AL
TIMD Aφ3 AL
TIMD Aφ2 AL
TIMD Aφ1 AL
TIMD Aφφ AL

TIMD CS IL
TIMD CAS IL
TIMD RAS BL

TIMD RAS PL



GND PIN 16
-5V PIN 1
+12V PIN 8
+5V PIN 9

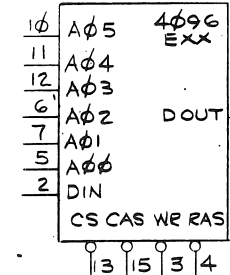
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
MSVII-C MOS MEMORY, LSI		D CS	M7955-0-1	B
SCALE		SHEET 7 OF 8	DIST.	

(ARRAY) DATA BITS (7-4) MTX2

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1-0-9962WSSD 2



GND PIN 16
-5V PIN 1
+12V PIN 8
+5V PIN 9

TIMD A05BL
TIMD A04BL
TIMD A03BL
TIMD A02BL
TIMD A01BL
TIMD A00BL

TIMD DI03H

TIMD CS0L
TIMD CAS0L
TIMD WB0L
TIMD RASDL

TIMD RASC L
TIMD A05AL
TIMD A04AL
TIMD A03AL
TIMD A02AL
TIMD A01AL
TIMD A00AL

TIMD CSI L
TIMD CAS1L
TIMD RASBL

TIMD RASAL

MTX3 03H

MTX3 02H

MTX3 01H

MTX3 00H

(ARRAY) DATA BITS (03-00) MTX3

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
MSV CMOS MEMORY, LSI		DCS	M7955-0-1	B
SCALE	SHEET	OF	DIST.	

