DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 2-13-76

TITLE KW11-K SYSTEM CHECKOUT AND ACCEPTANCE PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
Russ Hanian	23 Feb 76	A	SP	KW11-K-2	

SHEET 1 OF 3

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE KW11-K SYSTEM CHECKOUT AND ACCEPTANCE PROCEDURE

The KW11-K option consist of one multi-layer hex module, M7025. There are two tests for system checkout and acceptance of the KW11-K option. The KW11-K diagnostic (MAINDEC-11-DZKWK-A) (MD-DXKW0-A) and the KW11-K diagnostic module to the DEC-X11 System Exerciser. Since the AD11-K (12-bit A/D) option can run in conjunction with the KW11-K, there are two procedures that follow, only one should be used. Refer to the respective diagnostic for setup and starting procedure.

I KW11-K (stand-alone or no AD11-K)

Logic Test (starting address 200) of the KW11-K Diagnostic, with SR = 000000, must run without any error printout for a minimum of 15 minutes or 20 passes. An End Pass is printed at the end of each pass of the diagnostic.

The DEC-X11 System Exerciser with the KW11-K diagnostic module should run for a minimum of one half hour.

II KW11-K AND AD11-K

There are two jumpers (7010771) that are included with the AD11-K option. These jumpers are made up with Fast-On terminators. Both the AD11-K module (A009) and the KW11-K module (M7025) have two Fast-On connectors, indicated as tab 1 and tab 2. Tab 1 and tab 2 should be jumpered to tab 1 and tab 2 respectively. This ties the KW11-K Schmitt Trigger One to the AD11-K External Start input and ties the KW11-K Clock A Overflow to the AD11-K Clock Overflow input.

SIZE	CODE	NUMBER	REV
A	SP	KW11-K-2	

DEC FORM NO EN-01022-16-N370-(381)
DRA 108

SHEET 2 OF 3

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE KW11-K SYSTEM CHECKOUT AND ACCEPTANCE PROCEDURE

Logic Test of the KW11-K Diagnostic, with SR = 000000, must run without any error printout for a minimum of 15 mins, or 20 passes.

The DEC-X11 System Exerciser with the KW11-K diagnostic module should run for a minimum of 15 minutes without error.

Disable the KW11-K System Exerciser module. Setup the AD11-K System Exerciser module for KW11-K Overflows, which will start an A/D conversion. The DEC-X11 System Exerciser should run for a minimum of one half hour without error.

Testing The Schmitt Triggers and Event Outputs (OPTIONAL)

The KW11-K Diagnostic has five special tests, each with its own starting address. Each test requires certain pins on the H854 I/O connector to be connected together. Each test should run for a minimum of two minutes. The test and jumpers are listed below. Two short 30 AWG jumpers are needed to run these tests.

TEST	STARTING ADDRESS	JUMP PINS
STP2 output & ST1	210	V to LL
STP1 output & ST2	214	DD to BB
ST3 & ST3 output	220	V to T and L to LL
A Event Out	224	VV to LL
B Event Out	230	TT to LL

KW11-K

SIZE	CODE	NUMBER	REV
A	SP	KW11-K-2	

DEC FORM NO EN-01022-16-N370-(381)
DRA 108

SHEET 3 OF 3

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 8-MAR-76

TITLE M7025 CIRCUIT DESCRIPTION

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
Russ Hamlin 8 MAR 76	9 MAR 76	A	SP	KW11-K-5	

DEC 16(382) 1079N971
DRA 107

SHT 1 OF 7

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE M7025 CIRCUIT DESCRIPTION

The M7025 module is used in the KW11-K option, a dual programmable real time clock. The M7025 is a hex multi-layer module consisting of a Unibus interface, a 16-bit programmable clock with mode and rate controls, an 8-bit programmable clock with rate control, and oscillator with dividers.

The circuits to be described are referenced to prints D-CS-M7025-Ø-1, which consist of 10 sheets. Each sheet has a name description and an alpha-numeric identification (D1-D10). All signals are source prefixed with the alpha-numeric identification. For example, signal D1 LD STAT A H1 (load A status register high byte) is generated on sheet D1 which is titled Address Selection.

It is assumed that the reader is familiar with Unibus operation and is familiar with interpreting circuit schematics of logic and circuits so that detailed description is not necessary. The description given here is to familiarize the user with the M7025 circuits enough to identify a portion needing attention. It is recommended that the user read the KW11-K manual (EK-KW11K-OP-001).

There are two programmable clocks on the KW11-K designated as Clock A and Clock B. The 16-bit clock is Clock A and the 8-bit clock is Clock B. Signal designation will contain the lettering A or B to signify which clock is involved.

The Unibus interface consist of the device address decoding, interrupt logic and arbritration, and the Unibus signal receivers and drivers. On sheet D1 the bus address lines are received and gated with BUS MSYN (master sync) to decode D1 DEVICE H.

SIZE	CODE	NUMBER	REV
A	SP	KW11-K-5	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 2 OF 7

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE M7025 CIRCUIT DESCRIPTION

Address lines A5 through A12 are X-OR'ed with switches. This gives the capability of changing the base device address to avoid address conflicts with other options or KW11-K's. There are two flip-flop at the top center of D1. They are used to synchronize the processor to the KW11-K. At TPØ (reference figure 1 timing diagram) D1 DEV ENABLE will set if D1 DEVICE is true. D1 DEV ENABLE is gated with D1 DATA IN and D1 DATA OUT (decoded from the Unibus C lines) which are used to enable the read register decoder (E69) or the load register decoder (E67). At TP1 DEV ENB 2 sets which produces BUS SSYN if D1 NOP1 through D1 NOP 4 are not selected. The NOP's are used to prevent interreaction with the AD11-K option device address. The address lines A01 to A04 are decoded (E67 and E69) for a particular register. A0 and the "C" lines are decoded with the status register for byte operations. The interrupt logic and arbritration is located on sheet D2. Clock A and Clock B have their separate interrupt circuits and arbritration. However, Clock A takes priority over Clock B if interrupts occur simultaneously. In the upper left of sheet D2 is the interrupt for Clock A. If an overflow or Mode flag occurs with the A Interrupt Enable Set, or if a STP1 (Schmitt Triggerl) occurs with the ST1 Interrupt Enable Set, or if Data Bus bit 10 and load Status Register occurs, the D2 A INTR FLOP will set. This will cause a Bus Request out of the 8647 (E98), interrupt arbritrator. Since it is this device that is requesting the interrupt, the 8647 will not pass the Bus Grant (D1 BG IN).

SIZE	CODE	NUMBER	REV
A	SP	KW11-K-5	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 3 OF 7

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE M7025 CIRCUIT DESCRIPTION

When Bus Grant occurs a Bus sack is sent and D2 BBSY (A Bus Busy) is set. The Bus Request is taken off the Unibus and BUS INTR and the vector lines are put onto the Unibus. The vector address is switch selectable to avoid conflicts with other devices and is decoded with D2 B BBSY to decode a clock A or Clock B vector address. Since this interrupt is Clock A D2 B BBSY, is not true sending a logical zero for vector address line D04. When the CP accepts the vector address, it sends a BUS SSYN (Slave Sync) which clears the D2 A INTR flop and D2 A BBSY.

In the upper right of sheet D2 is the interrupt for Clock B. D2 B INTR sets if a B Overflow occurs with the B clock interrupt enable is set on if data Bit BD09 is true and a load B Status Register HI occurs. The interrupt operates in the same manner as Clock A interrupt. Here vector line D04 is sent a logical one to signify it's a clock B interrupt.

The Bus Data line receivers and drivers are on sheet D3 and D4. The registers which are readable are multiplexed and driven onto the Unibus by the 8838 (or 8641). The receiving of the Data Bus is also done by the 8838.

The Clock A Counter, Preset Buffer and Status register are located on sheet D7. The A Counter register is made up of 74193 cascading binary counters. D7 A Overflow (located at the top center) is true when the A Counter is all ones and count up pulse is present. The A Overflow is delayed and renamed D7 A Reload (located at the top right). This is used to re-clock the buffer data into the A Counter in modes Ø and 1. The A Buffer is made up of 74193 binary counters.

SIZE	CODE	NUMBER	REV
A	SP	KW11-K-5	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 4 OF 7

The count-down input is used to increment (2's compliment-decrement) the A Buffer data in Auto Increment Mode. Data to the A Buffer can be from the A Counter or the Buffered Data Bus. The A Buffer data is multiplexed by 74153, two to one line multiplexers. The B Clock Counter, Preset Buffer and Status registers are located on sheet D8. The B Counter is made up of 74193 binary counters. The Overflow from the counter is used to reload the counter with the data in the B Buffer is from the buffered data bus.

A 20 MHZ oscillator is used to generate timing pulses and various other frequencies that are a multiple of 20 MHZ. The 20 MHZ oscillator is located on the lower left of sheet D5, 74S124. It is divided by 74190 BCD counters to 1 MHZ, 100KHZ, 10KHZ, and 100HZ. These frequencies are decoded by a 74157 (multiplexer) to one frequency which is used to increment Clock A Counter. Clock B frequency dividers and multiplexer are located on sheet D9.

The four Schmitt Triggers are located on sheet **9** . Three of the Schmitt Triggers inputs have threshold control and slope control. The fourth Schmitt Trigger is used for line frequency (location B7). The outputs of Schmitt Triggers One, two and the line frequency are synchronized to the timing pulses produced on sheet D5. Refer to the timing chart in figure 1 for timing relationship. The resistor/diode network on the input of ST1, ST2 and ST3, is for protection and converting the input to Ø to +3V. The LM339 (E10) inputs cannot exceed +4V.

When the + input exceeds the - input, the output of the LM339 will go to +4V. When the + input becomes LESS than the - input, the output of the LM339 will go to ØV. The 1MΩ feedback resistor is for hysteresis. When the output of the LM339 is positive, 50 mV is fed back into the input. This is an effective ½V hysteresis at the resistor/diode network input.

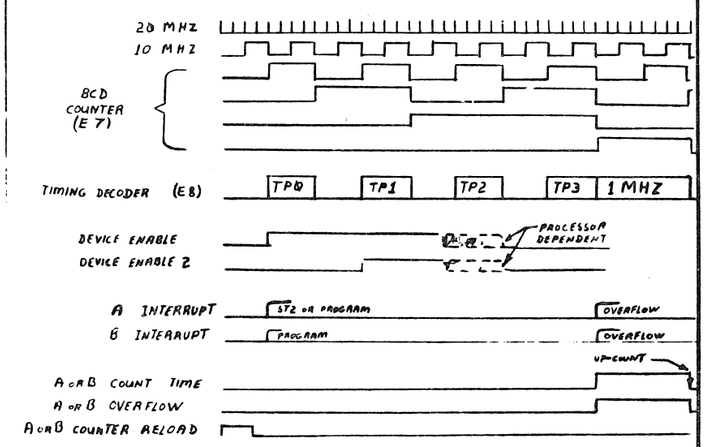
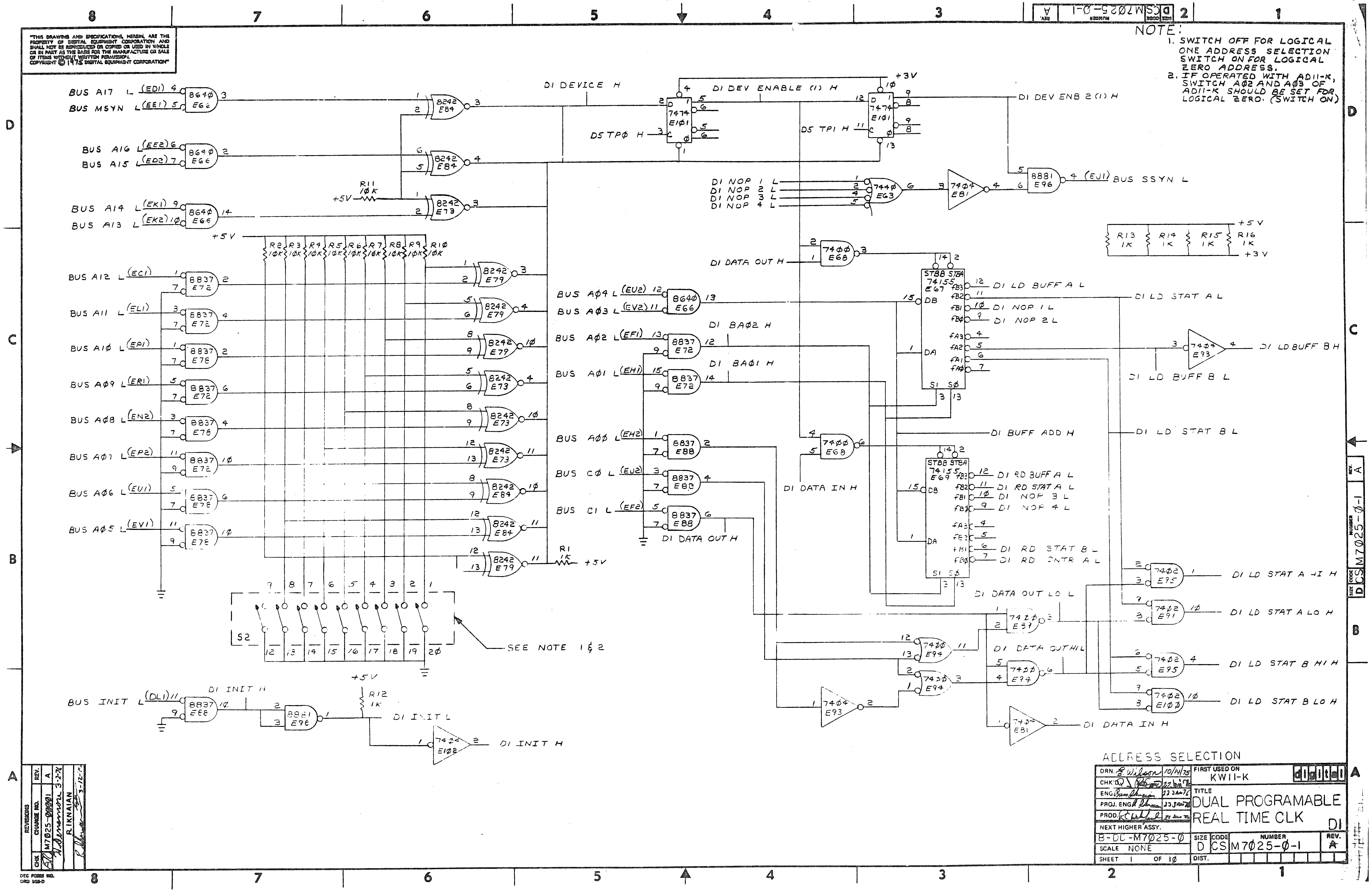


FIGURE 1 : TIMING DIAGRAM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NOTE:
1. SWITCH OFF FOR LOGICAL ONE ADDRESS SELECTION SWITCH ON FOR LOGICAL ZERO ADDRESS.
2. IF OPERATED WITH AD11-K, SWITCH A02 AND A03 OF AD11-K SHOULD BE SET FOR LOGICAL ZERO. (SWITCH ON)
BUS A17 L
BUS MSYN L
BUS A16 L
BUS A15 L
BUS A14 L
BUS A13 L
BUS A12 L
BUS A11 L
BUS A10 L
BUS A09 L
BUS A08 L
BUS A07 L
BUS A06 L
BUS A05 L
BUS A04 L
BUS A03 L
BUS A02 L
BUS A01 L
BUS A00 L
BUS C0 L
BUS C1 L
BUS INIT L
DI DEVICE H
DI DEV ENABLE (1) H
DI DEV ENB 2 (1) H
D5 TP0 H
D5 TP1 H
DI NOP 1 L
DI NOP 2 L
DI NOP 3 L
DI NOP 4 L
BUS SSYN L
DI DATA OUT H
DI LD BUFF A L
DI LD STAT A L
DI NOP 1 L
DI NOP 2 L
DI LD BUFF B H
DI LD BUFF B L
DI BA02 H
DI BA01 H
DI BUFF ADD H
DI LD STAT B L
DI DATA IN H
DI RD BUFF A L
DI RD STAT A L
DI NOP 3 L
DI NOP 4 L
DI RD STAT B L
DI RD CNTR A L
DI DATA OUT LO L
DI DATA OUT HI L
DI LD STAT A HI H
DI LD STAT A LO H
DI LD STAT B HI H
DI LD STAT B LO H
DI DATA IN H
DI INIT H
DI INIT L
DI INIT H
SEE NOTE 1 & 2
S2
ADDRESS SELECTION
DRN. Wilson 10/14/75
FIRST USED ON KW11-K
digital
TITLE DUAL PROGRAMABLE REAL TIME CLK
DI
NEXT HIGHER ASSY. B-DD-M7025-0
SCALE NONE
SHEET 1 OF 10
SIZE D CODE CS NUMBER M7025-0-1 REV. A
REVISIONS
M7025-00001
R. IKNAIAN
D CS M7025-0-1 A

NOTE:
3. VECTOR SWITCH SETTINGS: ON FOR A LOGIC "1" OFF FOR A LOGIC "Ø"
6. REMOVE W1 IN 11/15 & 11/20 WITHOUT KWII OPTION

D1 LD STAT B HI H
D4 BDØ9 H
D8 B INTR ENB (1) H
D8 B OVERFLOW H
D2 CLR INTR B H
D8 B INTR ENB (1) L
D2 B INTR (1) L
D2 B INTR (Ø) L

D1 LD STAT 9 HI H
D4 BD 1Ø H
D7 SET MODE FL L
D7 NEW A OVFL L
D7 A INTR ENB (1) H
D9 STPI-1 H
D7 STI INTR ENB (1) H
D2 CLR INTR A H
D7 STI INTR ENB (Ø) L
D7 A INTR ENB (Ø) L
+3V
D2 A INTR (1) H
D2 A INTR (1) L
D2 A INTR (Ø) H

SEE NOTE #6
W1
+5V
R17 1ØK
BUS NPR L (FJ1)
RQST
BG IN
BG OUT
SACK
SSYN
MASTER
CLR SACK
BBSY
MASTER CLR
BRQST
B647 E98
B647 E72
+5V
RG9 18Ø
D2 B BG IN H
D2 B SSYN L
7 (FT2) BUS SACK L
D2 A BBSY L
1Ø (FD1) BUS BBSY L
9 (DJ2) BUS REQUEST L
D2 B BG OUT H
D2 B BBSY L
D1 INIT H

BUS SSYN L (EJ1)
D2 A BBSY L
D2 A BBSY H
D2 CLR INTR A H
D2 CLR INTR B H
D2 A BBSY L
D2 B BBSY L

+3V
(CU2) BUS DØ2 L
(CN2) BUS DØ4 L
SEE NOTE 3
S1
(CT2) BUS DØ3 L
(CP2) BUS DØ5 L
(CV2) BUS DØ6 L
(CM2) BUS DØ7 L
(CL2) BUS DØ8 L
(FM1) BUS INTR L

+5V
R18 18Ø
R19 39Ø
R20 18Ø
D2 B BG IN H (DU2)
D2 B BG OUT H (DV2)
BUS BG4 OUT H (DT2)
BUS BG4 IN H (DS2)
BUS BG5 OUT H (DR2)
BUS BG5 IN H (DP2)
BUS BG6 OUT H (DN2)
PRIORITY JUMPER
E6Ø
LEVEL 6 STANDARD
16 (DD2) BUS BR7 L
15 (DE2) BUS BR6 L
14 (DF2) BUS BR5 L
13 (DH2) BUS BR4 L
12 (DJ2) BUS REQUEST L
11 (DK2) BUS BG7 IN H
1Ø (DL2) BUS BG7 OUT H
9 (DM2) BUS BG6 IN H

AA2 BA2 CA2 DA2 EA2 FA2 +5V
C3 THRU C46 .22µF
C47 THRU C52 15µF
AC2 BC2 CC2 DC2 EC2 FC2 AT1 BT1 CT1 DT1 ET1 FT1

INTERRUPT CONTROL

DRN. R Wilson	6/21/75	FIRST USED ON KWII-K	digital
CHK.		TITLE DUAL PROGRAMABLE REAL TIME CLK D2	
ENG.			
PROJ. ENG.			
PROD.			
NEXT HIGHER ASSY. B-DD-M7Ø25-Ø		SIZE D CODE CS NUMBER M7Ø25-Ø-1 REV. A	
SCALE NONE			
SHEET 2 OF 1Ø		DIST.	

REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 102-D

SIZE CODE D CS M7Ø25-Ø-1 REV. A

DEV ENABLE (1) L

STB 74151 E42
D8 CNTR BØ7 (1) H
D8 BUFF BØ7 (1) H
D8 OVERFLOW FL B (1) H
D7 CNTR AØ7 (1) H
D7 BUFF AØ7 (1) H
D7 MODE FLAG A (1) H
F1 5, FØ 6
S2 S1 SØ 9 10 11

8838 E37
(CM2) BUS DØ7 L
D3 BDØ7 H

STB 74151 E47
D8 CNTR BØ3 (1) H
D8 BUFF BØ3 (1) H
D8 RATE B2 (1) H
D7 CNTR AØ3 (1) H
D7 BUFF AØ3 (1) H
D7 RATE A2 (1) H

8838 E43
CT2 BUS DØ3 L
D3 BDØ3 H

D1 BUFF ADD H
D1 BA Ø2 H
D1 BA Ø1 H

STB 74151 E27
D8 CNTR BØ6 (1) H
D8 BUFF BØ6 (1) H
D8 B INTR ENB (1) H
D7 CNTR AØ6 (1) H
D7 BUFF AØ6 (1) H
D7 A INTR ENB (1) H

8838 E37
(CV2) BUS DØ6 L
D3 BDØ6 H

STB 74151 E46
D8 CNTR BØ2 (1) H
D8 BUFF BØ2 (1) H
D8 RATE B1 (1) H
D7 CNTR AØ2 (1) H
D7 BUFF AØ2 (1) H
D7 RATE A1 (1) H

8838 E43
(CV2) BUS DØ2 L
D3 BDØ2 H

STB 74151 E40
D8 CNTR BØ5 (1) H
D8 BUFF BØ5 (1) H
D8 FEED B TO A (1) H
D7 CNTR AØ5 (1) H
D7 BUFF AØ5 (1) H
D7 OVERFLOW FL A (1) H

8838 E37
(CP2) BUS DØ5 L
D3 BDØ5 H

STB 74151 E34
D8 CNTR BØ1 (1) H
D8 BUFF BØ1 (1) H
D8 RATE BØ (1) H
D7 CNTR AØ1 (1) H
D7 BUFF AØ1 (1) H
D7 RATE AØ (1) H

8838 E43
(CR2) BUS DØ1 L
D3 BDØ1 H

STB 74151 E36
D8 CNTR BØ4 (1) H
D8 BUFF BØ4 (1) H
D8 AUTO INC (1) H
D7 CNTR AØ4 (1) H
D7 BUFF AØ4 (1) H

8838 E37
(CN2) BUS DØ4 L
D3 BDØ4 H

STB 74151 E51
D8 CNTR BØØ (1) H
D8 BUFF BØØ (1) H
D8 ENB CNTR B (1) H
D7 CNTR AØØ (1) H
D7 BUFF AØØ (1) H
D7 ENB CNTR A (1) H

8838 E43
(CS2) BUS DØØ L
D3 BDØØ H

D1 DATA OUT H

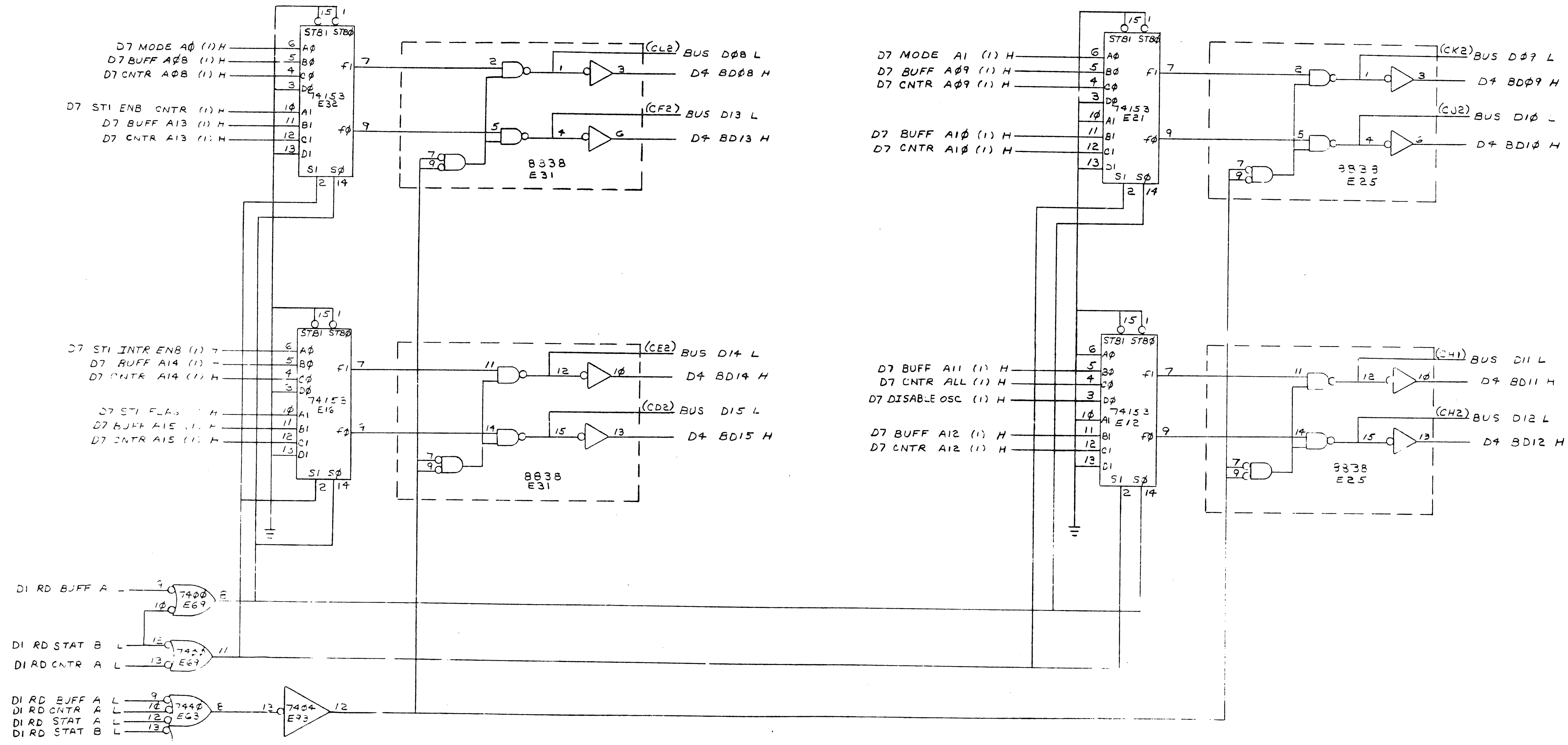
DATA BUS (ØØ-Ø7)

REVISIONS	REV.
CHANGE NO.	
CHK.	

DEC FORM NO. ORD 1020-0

DRN. E Wilson	10/20/76	FIRST USED ON KWII-K
CHK'D		digital
ENG.		
PROJ. ENG.		TITLE DUAL PROGRAMABLE REAL TIME CLK D3
PROD.		
NEXT HIGHER ASSY. B-DD-M7Ø25-Ø		SIZE D CODE CS NUMBER M7Ø25-Ø-1 REV. A
SCALE		DIST.
SHEET 3 OF 1Ø		

SIZE CODE DCS NUMBER M7Ø25-Ø-1 REV. A

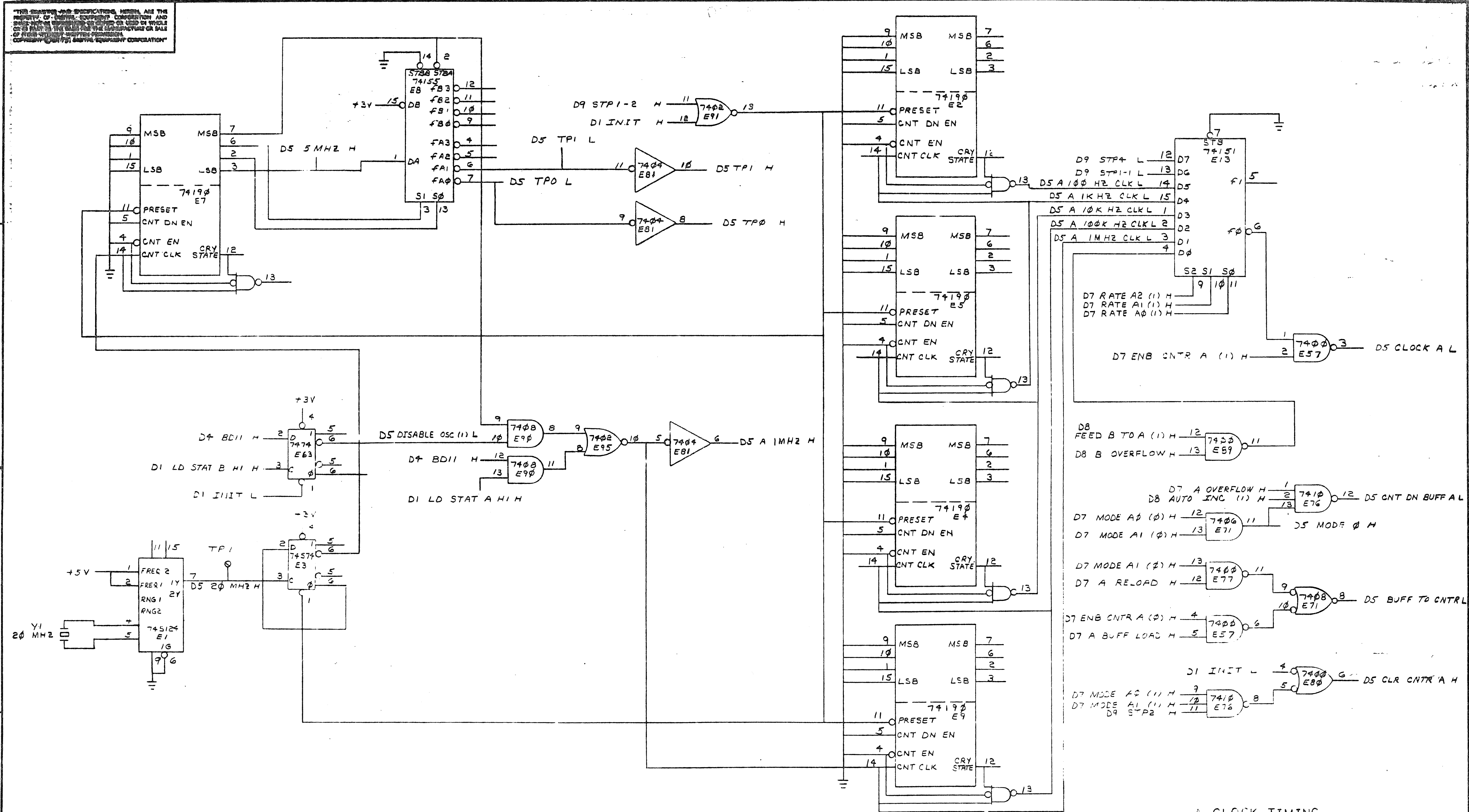


DATA BUS (Ø8-15)

DR. Ballison 10/23/75	FIRST USED ON KW11-K
CHK'D	TITLE
ENG	DUAL PROGRAMABLE
PROJ. ENG	REAL TIME CLK
PROD.	D4
NEXT HIGHER ASSY. 5-CC-M7Ø25-Ø	SIZE D CODE CS NUMBER M7Ø25-Ø-1 REV. A
SCALE NONE	
SHEET 4 OF 1Ø	DIST.

REVISIONS: REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 102-D



A CLOCK TIMING

DR	[signature] 10/27/75
CHK'D	[signature]
ENG	[signature]
PROJ. ENGR	[signature]
PROD	[signature]
FIRST USED ON	KW11-K
TITLE	DUAL PROGRAMABLE REAL TIME CLK D5
NEXT HIGHER ASSY.	B-CD-M7Ø25-Ø
SIZE / CODE / NUMBER / REV	D CS M7Ø25-Ø-1 A
SCALE	NONE
SHEET	5 OF 1Ø

D8 FEED B TO A (1) L
D9 STP 1-2 L
D1 INIT H
74Ø2 E91

D5 A 1MHZ H
D8 FEED B TO A (1) H
D8 FEED B TO A (Ø) H
74Ø8 E9Ø
74Ø2 E82
DG B 1MHZ L

MSB LSB
74191Ø
PRESET
CNT DN EN
CNT EN
CNT CLK
CRY STATE
E97

+3V
TP2
74S74 E3
D5 2Ø MHZ H

E65 — DG B 1ØØ HZ L
E59 — DG B 1KHZ L
E53 — DG B 1Ø KHZ L
E48 — DG B 1ØØKHZ

STB
74151 E58
D9 STP4 L
D9 ST3 L
+3V
D7 D6 D5 D4 D3 D2 D1 DØ
S S1 SØ
F1
FØ
74ØØ E7Ø
DG CLOCK B L
D8 ENB CNTR B(1) H
D8 RATE B2 (1) H
D8 RATE B1 (1) H
D8 RATE BØ (1) H

B CLOCK TIMING

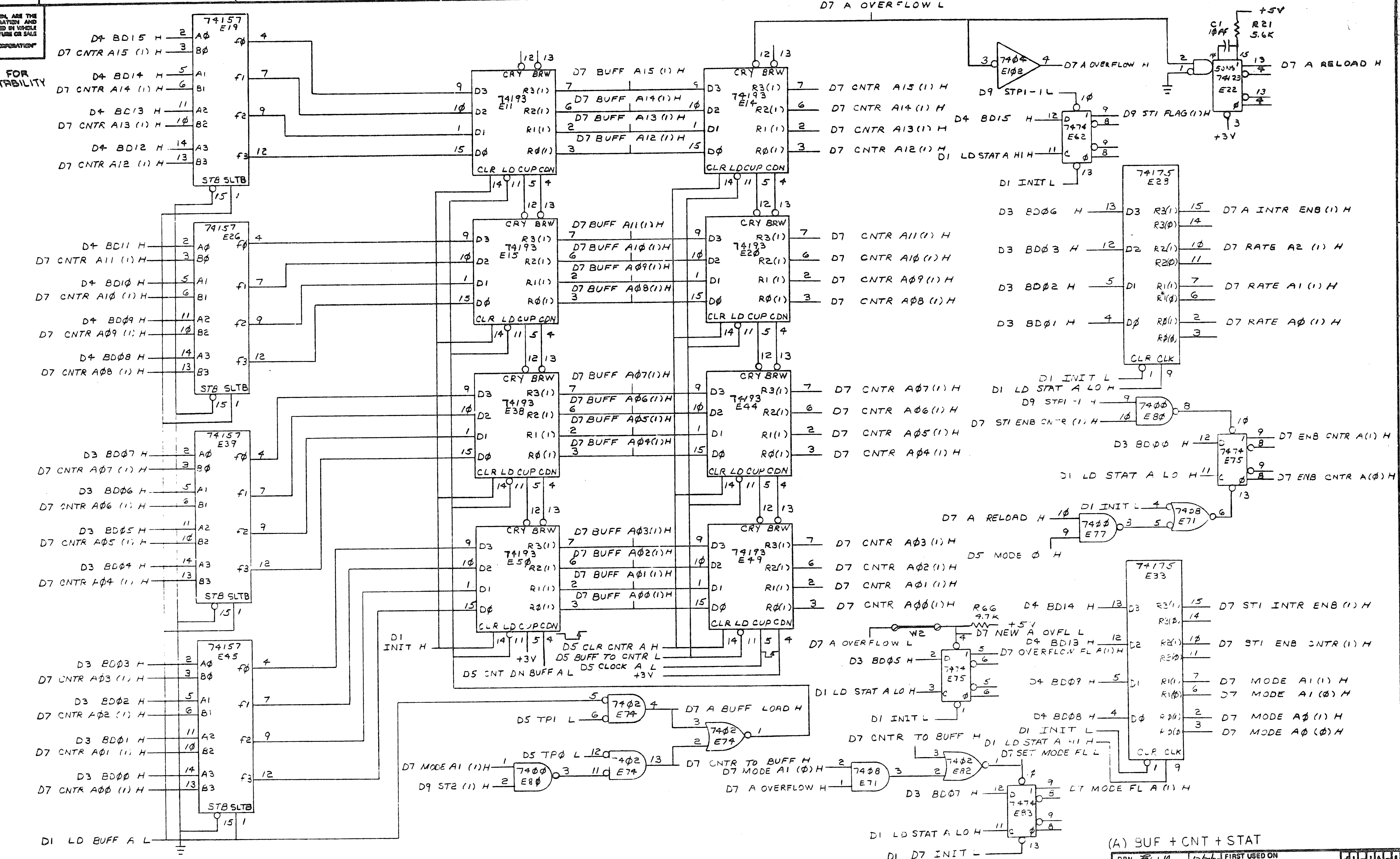
DRN.		10/20/75	FIRST USED ON KW11-K
CHK'D		22 Jan 76	
ENG		22 Jan 76	TITLE DUAL PROGRAMABLE REAL TIME CLK D6
PROJ. ENG		22 Jan 76	
PROD.		21 Jan 76	
NEXT HIGHER ASSY.	B-DD-M7025-Ø		SIZE D CODE CS NUMBER M7Ø25-Ø-1 REV. A
SCALE NONE			
SHEET 6 OF 1Ø			DIST.

REVISIONS: REV. | CHANGE NO. | CHK

DEC PERRIS P/A. DRD 10 -D

SIZE D CODE CS M7Ø25-Ø-1 REV. A

NOTE: 1. REMOVE W2 FOR LPS11 COMPATABILITY



(A) BUF + CNT + STAT

FIRST USED ON	KW11-K
TITLE	DUAL PROGRAMBLE REAL TIME CLK D7
NEXT HIGHER ASSY.	B-DD-M7025-0
SIZE / CODE / NUMBER / REV.	D CS M7025-0-1 A
SCALE	NONE
SHEET	7 OF 10

D8 B OVERFLOW L

+5 V

C2 10pf

R22 5.6K

74123 E22 50NS

D8 * B RELOAD H

D8 B RELOAD L

+3V

74Ø4 E16Ø

D8 B OVERFLOW H

D8 B OVERFLOW L

74Ø4 E83

D3 BDØ7 H

D8 OVERFLOW FL B (1) H

D1 LD STAT B LO H

D1 INIT L

74175 E41

D3 BDØ7 H

D3 BDØ6 H

D3 BDØ5 H

D3 BDØ4 H

D8 BUFF BØ7 (1) H

D8 BUFF BØ6 (1) H

D8 BUFF BØ5 (1) H

D8 BUFF BØ4 (1) H

74193 E3Ø

CRY BRW

D8 CNTR BØ7 (1) H

D8 CNTR BØ6 (1) H

D8 CNTR BØ5 (1) H

D8 CNTR BØ4 (1) H

74175 E29

D3 BDØ6 H

D3 BDØ3 H

D3 BDØ2 H

D3 BDØ1 H

D8 B INTR ENB (1) H

D8 B INTR ENB (1) L

D8 RATE B2 (1) H

D8 RATE B1 (1) H

D8 RATE BØ (1) H

D1 INIT L

D1 LD STAT B LO H

74175 E35

D3 BDØ3 H

D3 BDØ2 H

D3 BDØ1 H

D3 BDØØ H

D8 BUFF BØ3 (1) H

D8 BUFF BØ2 (1) H

D8 BUFF BØ1 (1) H

D8 BUFF BØØ (1) H

74193 E52

D8 CNTR BØ3 (1) H

D8 CNTR BØ2 (1) H

D8 CNTR BØ1 (1) H

D8 CNTR BØØ (1) H

+3V

D6 CLOCK B L

D1 INIT L

D1 LD BUFF B H

D1 INIT H

74175 E64

D3 BDØØ H

D3 BDØ4 H

D3 BDØ5 H

D8 ENB CNTR B (1) H

D8 ENB CNTR B (Ø) H

D8 AUTO INC (1) H

D8 FEED B TO A (1) H

D8 FEED B TO A (1) H

D9 STPI - 2 H

D8 FEED B TO A (1) H

74ØØ E7Ø

D8 B RELOAD L

7410 E72

74Ø4 E1Ø2

D8 ENB CNTR B (Ø) H

D5 TPI H

74ØØ E7Ø

REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 102-D

'B' BUFF + CNT + STAT

DRN. E Wilson	11/3/75	FIRST USED ON KW11 K
CHK. [illegible]	22 Jan 76	
ENG. [illegible]	22 Jan 76	TITLE DUAL PROGRAMABLE REAL TIME CLK D8
PROJ. ENG. [illegible]	22 Jan 76	
PROD. KC Wilson	21 Jan 76	
NEXT HIGHER ASSY. E-DD-M7025-Ø		SIZE D CODE CS NUMBER M7025-Ø-1 REV. A
SCALE NONE		
SHEET 8 OF 1Ø		DIST.

NOTE: 5. W3, W4 & W5 ARE PLACED FOR TTL INPUTTING.

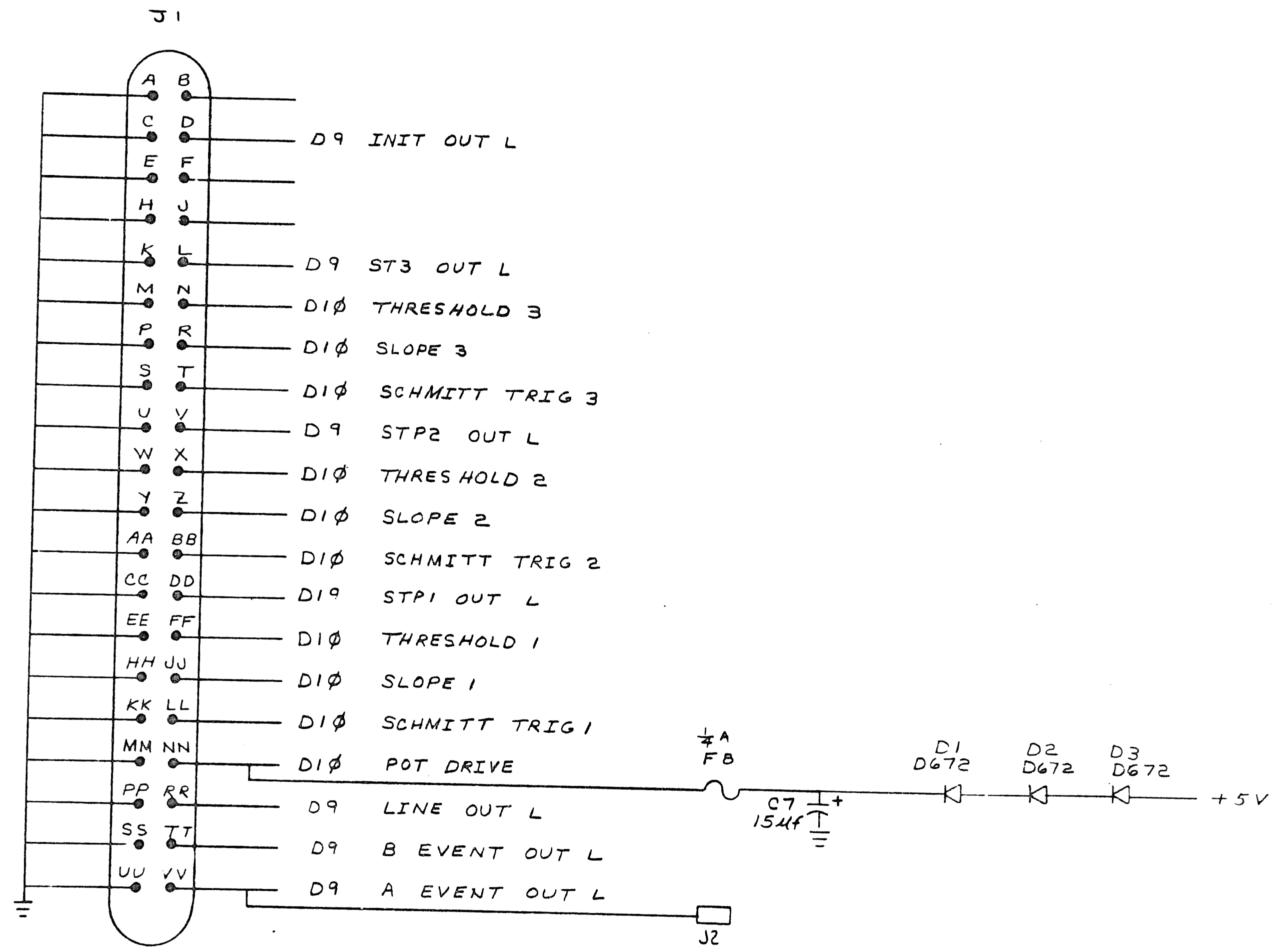
D1 LD STAT A HI H
D4 BD1Ø H
D1Ø SCHMITT TRIG
D1Ø THRESHOLD (Ø TO +3V)
D1Ø SLOPE 2
D1Ø SCHMITT TRIG
D1Ø THRES HOLD (Ø TO +3V)
D1Ø SLOPE 1
LTC L (CD1)
D1Ø SCHMITT TRIG
D1Ø THRESHOLD (Ø TO +3V)
D1Ø SLOPE 3
D4 BD12 H
D1 LD STAT A HI H
D9 ST2 H
D9 ST2(1) L
D9 ST2 (1) H
D5 TP1 L
D1 INIT L
D9 STP2 H
D9 STP2 OUT L
D5 A 1MHZ H
D9 STP1-1 L
D9 STP1-1 H
D9 ST1 (1) H
D9 STP1 OUT L
D8 AUTO INC (1) H
D9 STP1-2 (1) H
D9 STP1-2 (1) L
D5 2ØMHZ H
D5 MODE Ø H
D9 ST1 H
D8 B OVERFLOW L
D9 B EVENT OUT L
D9 STP4 L
D9 ST4 (1) H
D9 ST4 (1) L
D9 LINE OUT L
D1 INIT L
D9 INIT OUT L
D7 A OVERFLOW L
D7 A EVENT OUT L
D9 ST3 H
D9 ST3 L
D9 ST3 OUT L

EXTERNAL INPUTS/OUTPUTS

DRN. E. Wilson	11/4/75	FIRST USED ON KW11-K	digital A
CHK.		TITLE DUAL PROGRAMABLE REAL TIME CLK D9	
ENG.			
PROJ. ENG.			
PROD.			
NEXT HIGHER ASSY. B-DD-M7Ø25-Ø		SIZE D CODE CS NUMBER M7Ø25-Ø-1 REV. A	
SCALE NONE			
SHEET 9 OF 1Ø		DIST.	

REVISIONS: REV. | CHANGE NO. | CHK

DEC FORM# RD. DRD 102-0



CABLING

DRN. E Wilson	11/5/75	FIRST USED ON	KW11-K
CHK'D		TITLE	DUAL PROGRAMABLE REAL TIME CLK D1Ø
ENG.	22 Jan 76		
PROJ. ENG.	22 Jan 76		
PROD.	21 Jan 76		
NEXT HIGHER ASSY. B-DD-M7Ø25-Ø		SIZE D CODE CS NUMBER M7Ø25-Ø-1	REV. A
SCALE NONE			
SHEET 1Ø OF 1Ø		DIST.	

digital

D CS M7Ø25-Ø-1 A

REVISIONS CHANGE NO. CHK REV.

DEC FORM NO. DRD 102-0

NOTES:

1. FOR DRAWING DIRECTORY, REFER TO: B-DD-M7825-0
2. WIRE ADD #27 IS TO BE INSTALLED AFTER GR MODULE TEST. ADD WIRE FROM E1(7) TO E3(11).

ETCH CUTS SIDE #1 AS SHOWN

1. CUT ETCH AT E97(8)
2. CUT ETCH AT PTH ABOVE E18(8)
3. CUT ETCH FROM S2(9)
4. CUT ETCH AT PTH TO LEFT OF E78(5/6)
5. CUT ETCH AT E78(14)
6. CUT ETCH AT PTH ABOVE FINGER E81.
7. CUT ETCH BETWEEN (2) AND (12) E100.
8. CUT ETCH E92(14).
9. CUT ETCH NEXT TO E98(2).
10. CUT ETCH AT E1(7).

ETCH CUTS SIDE #2 AS SHOWN

1. CUT ETCH AT PTH TO RIGHT OF E24 (1 & 2)
2. CUT ETCH AT PTH FROM E22(4)
3. CUT ETCH AT E22(2)
4. CUT ETCH AT PTH BETWEEN E22(6 & 11)
5. CUT ETCH AT E22(7)
6. CUT ETCH AT E97(9)
7. CUT ETCH AT PTH FROM E87(8)
8. CUT ETCH FROM E78(13)
9. CUT ETCH TO RIGHT OF S2(9)
10. CUT ETCH BELOW & TO LEFT OF S2(11)
11. & 12. CUT ETCH BOTH SIDES OF E100(12)
13. CUT ETCH AT E92(15).
14. CUT ETCH AT E98(15).

WIRE ADDS SIDE #1 AS SHOWN

1. ADD WIRE FROM E103(1) (SPARE LOCATION) TO E98(6)
2. ADD WIRE FROM E91(11) TO PTH TO RIGHT OF E87(14)
3. ADD WIRE FROM PTH TO RIGHT OF E87(14) TO E87(9)
4. ADD WIRE FROM E87(1) TO E97(9)
5. ADD WIRE FROM PTH TO LEFT OF E24(1 & 2) TO PTH ABOVE E18(8)
6. ADD WIRE FROM PTH TO LEFT OF E24(1 & 2) TO E22(2)
7. ADD WIRE FROM E22(1) TO E22(8)
8. ADD WIRE FROM E22(8) TO C2 (LOWER LEAD)
9. ADD WIRE FROM E22(7) TO R22 (LOWER LEAD)
10. ADD WIRE FROM E22(13) TO SECOND PTH ABOVE AND TO LEFT OF E22(1)
11. ADD WIRE FROM R2 (LOWER LEAD) TO E79(12)
12. ADD WIRE FROM E79(12) TO E79(13)
13. ADD WIRE FROM PTH BELOW & TO RIGHT OF S2(11) TO E78(11)
14. ADD WIRE FROM PTH BELOW & TO LEFT OF C35 TO E66(12)
15. ADD WIRE FROM PTH TO LEFT OF E78(5/6) TO E66(11)
16. ADD WIRE FROM E66(13) TO PTH TO LEFT OF E67(1)
17. ADD WIRE FROM E100(2) TO E29(14)
18. ADD WIRE FROM E100(12) TO E82(13)
19. ADD WIRE FROM PTH TO RIGHT OF E102(12) TO PTH BETWEEN R9 & R10
20. ADD WIRE FROM E85(2) TO E82(11)
21. ADD WIRE FROM E82(12) TO PTH ABOVE E75(1)
22. ADD WIRE FROM E93(6) TO E92(14).
23. ADD WIRE FROM E93(9) TO E98(11).
24. ADD WIRE FROM E93(8) TO E96(14).
25. ADD WIRE FROM E98(15) TO PTH UNDER C52.
26. ADD WIRE FROM E92(15) TO PTH UNDER C52.
27. SEE NOTE #2.

COMPONENT ADDS SIDE #1 AS SHOWN

1. ADD RESISTOR (R69) BETWEEN SPARE LOCATION E103(1 & 16)

DEC 8647	8	16
DEC 2501-00	14	1
DEC 8838	8	16
DEC 8837	8	16
DEC 8640	1	8
DEC 74S124	8	16
DEC 75453	4	8
DEC 74193	8	16
DEC 74190	8	16
DEC 74175	8	16
DEC 74157	8	16
DEC 74155	8	16
DEC 74153	8	16
DEC 74151	8	16
DEC 74123	8	16
LM339	12	3
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO
2	E71,E90	I.C. DEC 7408	1910155	50
3	E77,E78,E88	I.C. DEC 8837	1911116	51
3	E73,E79,E84	I.C. DEC 8242	1909712	52
5	E74,E82,E91,E95,E100	I.C. DEC 7402	1909004	53
1	E76	I.C. DEC 7410	1905576	54
3	E81,E93,E102	I.C. DEC 7404	1909686	55
2	E92,E98	I.C. DEC UNIBUS INTERRUPT CHIP(8647)	1912083	56
2	W1,W2	JUMPER, #22 AWG (INSULATED)	9009185	57
10		SPLIT LUGS	9006735	58
2	J2,J3	OFFSET FASTON TAB	9007112	59
2		EYELET (FOR FASTON)	9007827	60
12		EYELET (HANDLE)	9006732	61
1		HANDLE ASSY.	1210711-02	62
1	E60	PRIORITY JUMPER LEVEL #6	5406780	63
1	(S1)	SWITCH COVER	1211284-01	64
1	(S2)	SWITCH COVER	1211284-06	65
A/R		WIRE 30 AWG GRN	9105740-55	66

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1		ETCHED CIRCUIT BOARD	5011007	1
2	C1,C2	CAP. 10pf 100V 5%	1000008	2
10	C3,C4,C6,C7,C47 THRU C52	CAP. 15uf 20V 10%	1004012	3
1	C5	CAP. .01uf 100V 20%	1001010-01	4
39	C8 THRU C46	CAP. .22uf 50V	1010274	5
3	D1,D2,D3	DIODE D672	1105275	6
2	D4,D5	DIODE ARRAY DEC 2501-00	1910010-00	7
8	F1 THRU F8	250MA PICO FUSE	1210929-04	8
1	J1	40 PIN BERG CONNECTOR	1209941-02	9
1		LATCH, R.H. FOR BERG CONN.	1209941-04	10
1		LATCH, L.H. FOR BERG CONN.	1209941-03	11
1	S1	SWITCH PACK (10 PIN)	1211164-01	12
1	S2	SWITCH PACK (20 PIN)	1211164-08	13
16	R2 THRU R11,R17,R32,R41, R48,R57	RES. 10K 5% ¼W	1300479	14
10	R12 THRU R16,R31,R37,R45, R53,R1	RES. 1K 5% ¼W	1300365	15
3	R18,R20,R69	RES. 180 5% ¼W	1301322	16
1	R19	RES. 390 5% ¼W	1300309	17
2	R21,R22	RES. 5.6K 5% ¼W	1301874	18
3	R24,R33,R49	RES. 100K 5% ¼W	1302466	19
3	R25,R34,R50	RES. 2K 5% ¼W	1302398	20
6	R26,R29,R35,R51,R55,R39	RES. 33K 10% ¼W	1300510	21
4	R27,R36,R44,R52	RES. 1M 5% ¼W	1309595	22
7	R28,R30,R38,R40,R43,R54,R56	RES. 15K 5% ¼W	1300496	23
1	R46	RES. 20K 5% ¼W	1302391	24
1	R47	RES. 62K 5% ¼W	1304840	25
7	R58 THRU R64	RES. 220 5% ¼W	1300271	26
3	R65,R67,R68	RES. 47 1% ¼W (FUSIBLE)	1310891-02	27
2	R42,R66	RES. 4.7K 5% ¼W	1300447	28
1	Y1	CRYSTAL 20MHZ	1809880	29
1	E1	I.C. DEC 74S124	1911911	30
10	E2,E4,E5,E7,E9,E49,E53, E59,E65,E97	I.C. DEC 74190	1910095	31
2	E3,E87	I.C. DEC 74S74	1910544	32
1	E6	I.C. DEC 7486	1910011	33
3	E8,E67,E89	I.C. DEC 74155	1910656	34
1	E10	I.C. DEC LM339N	1912108	35
10	E11,E14,E15,E20,E30,E39, E44,E48,E50,E52	I.C. DEC 74193	1910018	36
4	E12,E16,E21,E32	I.C. DEC 74153	1909937	37
10	E13,E27,E34,E36,E40,E42, E46,E47,E51,E58	I.C. DEC 74151	1909936	38
4	E17,E18,E23,E24	I.C. DEC 75453	1911036	39
4	E19,E26,E39,E45	I.C. DEC 74157	1910655	40
1	E22	I.C. DEC 74123	1910436	41
4	E25,E31,E37,E43	I.C. DEC 8838	1911117	42
6	E28,E29,E33,E35,E41,E64	I.C. DEC 74175	1910651	43
3	E54,E55,E96	I.C. DEC 8881	1909705	44
8	E56,E61,E62,E75,E83,E86, E99,E101	I.C. DEC 7474	1905547	45
8	E57,E68,E70,E77,E80,E85, E89,E94	I.C. DEC 7400	1905575	46
1	[illegible]	I.C. SOCKET, 16 PIN (PRIORITY JUMPER)	1209839	47
1	E63	I.C. DEC 7440	1905579	48
1	E66	I.C. DEC 8640	1911469	49

FIRST USED ON OPTION MODEL: KM11-K

PARTS LIST

ETCH BOARD REV.

REV.	CHG	CHANGE NO.	REVISIONS
A		M7025-00001	12-MAR-76 R.J.NAIGAN

DEC NO. | EIA NO. | DEC NO. | EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN.	E. Wilson	DATE 11/5/75
CHKD.	[illegible]	DATE 22 Jan 76
ENG.	[illegible]	DATE 22-Jan-76
PROJ. ENG.	[illegible]	DATE 22 Jan 76
PROD. ENG.	[illegible]	DATE 22-Jan-76

NEXT HIGHER ASSY: B-DD-M7025-0

SCALE: NONE

SHEET 1 OF 4

digital

TITLE: DUAL PROGRAMABLE REAL TIME CLK

SIZE	CODE	NUMBER	REV.
D	UA	M7025-0-0	A

DIST.

NOTES:

SIGNATURES	DATE
DRN. E Wilson	11/5/75
CHK D.P	22 Jan 76
ENG	22 Jan 76
PROJ. ENG	22 Jan 76
PROD	21 Jan 76
SCALE 2/1	
SHT. 2 OF 4	
ETCH REV	

digital

TITLE
DUAL PROGRAMABLE REAL TIME CLK

SIZE	CODE	NUMBER	REV
D	UA	M7Ø25-Ø-Ø	A

FIRST USED ON KW11-K

1 MS#30204