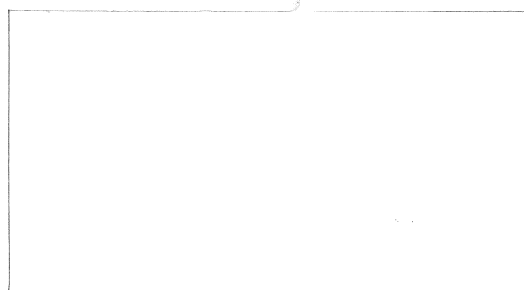


pdp11

DL11
asynchronous
line interface
engineering drawings

digital



**DL11
asynchronous
line interface
engineering drawings**

digital equipment corporation • maynard, massachusetts

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET

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SEQUENCE

SEQUENCE

PRINT SET #1

DRAWING DIRECTORY B-DD-DL11-0
ASYNCHRONOUS LINE INTERFACE C-UA-DL11-0-0
ASYNCHRONOUS LINE INTERFACE (PL) A-PL-DL11-0-0
ASYNCHRONOUS LINE INTERFACE E-CS-M7800-0-1
CABLE ASSEMBLY (KLB/E) D-1A-7008360-0-0
SOFTWARE LIST A-SL-DL11-0-4
ACCESSORY LIST A-AL-DL11-0-5
INSTALLATION PROCEDURE A-SP-DL11-0-2

PRINT SET #3

DRAWING DIRECTORY B-DD-DL11-0
ASYNCHRONOUS LINE INTERFACE C-UA-DL11-0-0
ASYNCHRONOUS LINE INTERFACE (PL) A-PL-DL11-0-0
ASYNCHRONOUS LINE INTERFACE E-CS-M7800-0-1
CABLE, MODEM BC05C D-UA-BC05C-0-0
CABLE ASSEMBLY (KLB/E) D-1A-7008360-0-0
MODEM TEST CONN. D-CS-H315-0-1
INSTALLATION PROCEDURE A-SP-DL11-0-2

PRINT SET #2

DRAWING DIRECTORY B-DD-DL11-0
ASYNCHRONOUS LINE INTERFACE C-UA-DL11-0-0
ASYNCHRONOUS LINE INTERFACE (PL) A-PL-DL11-0-0
ASYNCHRONOUS LINE INTERFACE E-CS-M7800-0-1
CABLE, MODEM BC05C D-UA-BC05C-0-0
FILTER NETWORK B-CS-G0000-0-1
MODEM TEST CONN. D-CS-H315-0-1
SOFTWARE LIST A-SL-DL11-0-4
ACCESSORY LIST A-AL-DL11-0-5
INSTALLATION PROCEDURE A-SP-DL11-0-2

UNIT VARIATIONS

PRINT SET TYPE

VARIATION

TITLE

VARIATION	TITLE
DL11-A	ASYNCHRONOUS LINE INTERFACE, CURRENT LOOP
DL11-B	ASYNCHRONOUS LINE INTERFACE, EIA
DL11-C	ASYNCHRONOUS LINE INTERFACE, CURRENT LOOP
DL11-D	ASYNCHRONOUS LINE INTERFACE, EIA
DL11-E	ASYNCHRONOUS LINE INTERFACE, DATA SET

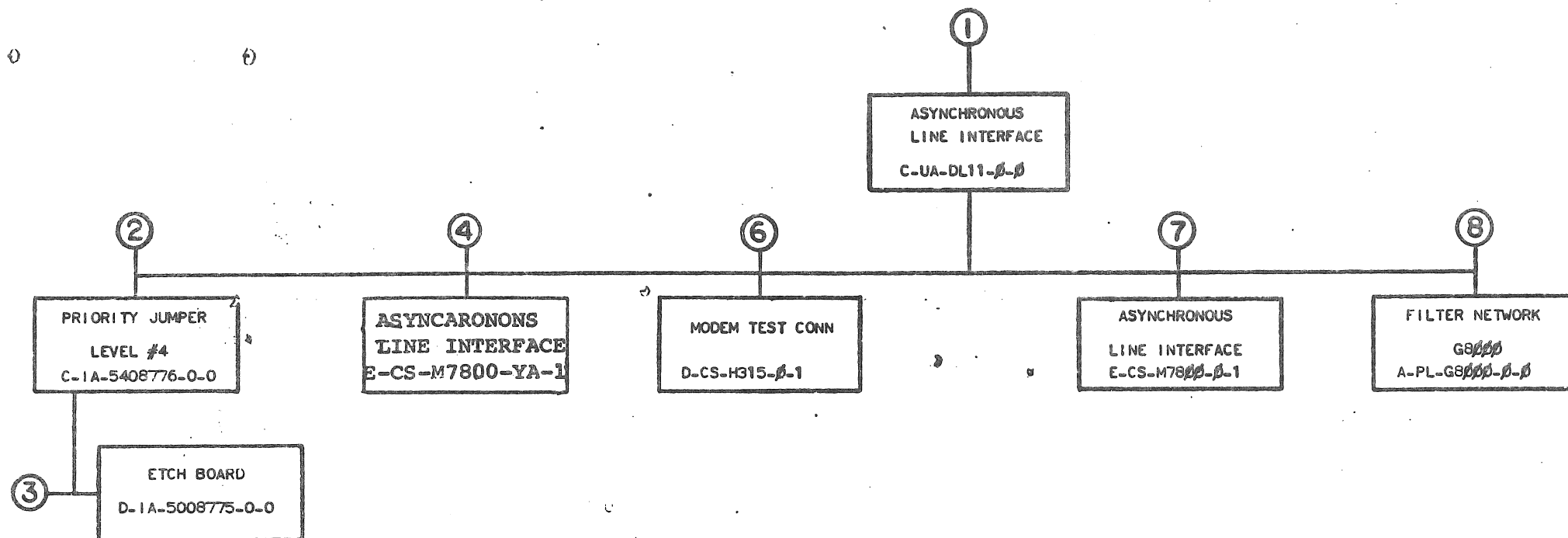
DL11-1	DL11-2
1	0
0	1
1	0
0	1
0	1

REVISIONS		DATE	CHG. NO.	REV
				A
				B
				C
				D
				E
				F

USED ON OPTION/MODEL	DRN.	DATE	TITLE
	M. Pierce	4-28-72	ASYNCHRONOUS LINE INTERFACE
	R. Cook	5/9/72	
	P. E. Janson	5/11/72	
	P. E. Janson	5/15/72	
	P. E. Janson	5/15/72	

SIZE	CODE	NUMBER	REV
B	DD	DL11-0	F

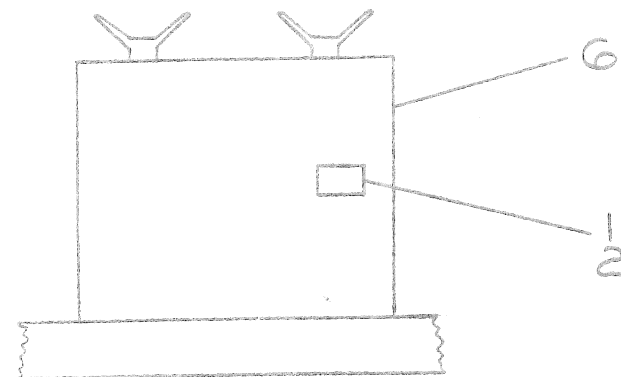
SHEET	OF	DIST
1	3	G



TITLE	SHEET	SIZE	CODE	NUMBER	REV
ASYNCHRONOUS LINE INTERFACE	2 OF 3	B	DD	DL11 - Ø	F

[illegible]

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1972



NOTES:

1. G 8000 IS REQUIRED ONLY IN PDP 11 SYSTEMS WHERE +15V IS NOT AVAILABLE. THE INSTALLATION REQUIRES 2 WIRES TO BE ADDED.

A03V2-A02V2

A02N2-CXXUI

WHERE (XX) IS THE SLOT NUMBER CONTAINING THE DLII.

2. ITEMS INDICATED WITH ASTERICK (*) ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THIS UNIT.

	A	B	C	D	E	F
4	M920 * UNIBUS OUT			G727 *		
3	G772 * POWER CONNECTOR			G727 *		
2	G8000 FILTER NETWORK SEE NOTE 1			G727 *		
1	M920 * UNIBUS IN			M7800 / M7800-YA		

DDII-A *

SEE NOTE 2

REV.	CHANGE NO.	REV.
A	DLII-00001	A
B	DLII-00002	B
C	DLII-00005	C
D	DLII-00006	D
E	DLII-00007	E
F	DLII-00008	F
G	DLII-00009	G
H	DLII-00010	H
I	DLII-00011	I
J	DLII-00012	J
K	DLII-00013	K
L	DLII-00014	L
M	DLII-00015	M
N	DLII-00016	N
O	DLII-00017	O
P	DLII-00018	P
Q	DLII-00019	Q
R	DLII-00020	R
S	DLII-00021	S
T	DLII-00022	T
U	DLII-00023	U
V	DLII-00024	V
W	DLII-00025	W
X	DLII-00026	X
Y	DLII-00027	Y
Z	DLII-00028	Z

FIRST USED ON OPTION/MODEL PDP-11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	DRN. M. Riva	DATE 7/18/72	digital EQUIPMENT CORPORATION WAYNARD, MASSACHUSETTS	
DECIMALS	CHK'D. J. F. Janson	DATE 4-29-72	TITLE ASYNCHRONOUS LINE INTERFACE	
ANGLES	ENG. J. F. Janson	DATE 5-11-72	SIZE CODE C UA	
.XXX = .005	PROD. J. F. Janson	DATE 5-15-72	NUMBER DLII-0-0	
.XX = .02			REV. D	
.X = .1				
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	NEXT HIGHER ASSY. B-00-DLII-0	SCALE NONE	DIST G	
MATERIAL + + +	SHEET OF			
FINISH + + +				

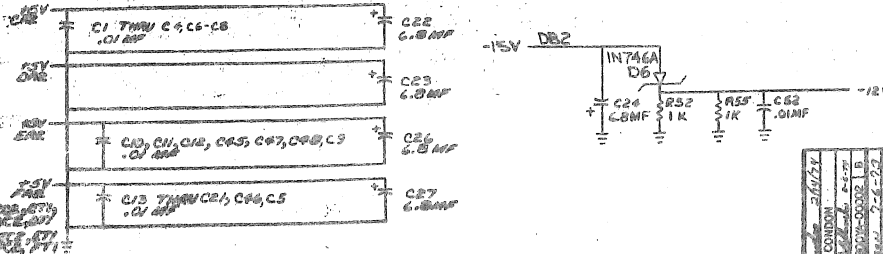
DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

MADE BY M. PIERCE	CHECKED J. FERGUSON	SECTION 1
DATE 4/27/72	DATE 4/27/72	ISSUED SECT. 1
ENG P. E. Johnson	PROD J. Mc Sique	
DATE 5/11/72	DATE 5/15/72	

QUANTITY / VARIATION

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	DL	DL	DL	DL	DL												
1	C-IA-5408776-0-0	PRIORITY JUMPER LEVEL #4	1	1	1	1	1												
2	C-IA-5408778-0-0	PRIORITY JUMPER LEVEL #5	-	-	-	-	-												
3	D-UA-BC05C-25	CABLE, MODEM BC05C	-	1	-	1	1												
4	D-IA-7008360-0-0	CABLE ASSEMBLY (KL8E)	1	-	1	-	-												
5	D-CS-H315-0-1	MODEM TEST CONNECTOR	-	-	-	-	A/R	See Note 2											
6	E-CS-M7800-0-1	ASYNCHRONOUS LINE INTERFACE	-	1	-	1	1												
7	A-PL-G8000-0-0	FILTER NETWORK	-	A/R	-	A/R	A/R	See Note 1											
8		CRYSTAL	A/R	A/R	A/R	A/R	A/R	See Note 3											
9	E-CS-M7800-YA-1	ASYNCHRONOUS LINE INTERFACE	1	-	1	-	-												
	NOTES:	1. G8000 IS REQUIRED ONLY IN PDP 11																	
		SYSTEMS WHERE +15V IS NOT																	
		AVAILABLE. ONE PER DD11-A.																	
		2. ONE H315 PER PDP11 SYSTEM																	
		3. CRYSTAL FREQUENCY DEFINED BY CUSTOMER																	
		SPECIFIED BAUD RATE																	
		4. APPLY TAPE TO TOP SURFACES OF CRYSTAL																	
		AND MOUNTING BRACKETS TO INSULATE FROM																	
		ADJACENT MODULES.																	
10	-9008269	TRANSPARENT VINYL TAPE	A/R																

TITLE ASYNCHRONOUS LINE INTERFACE	ASSY NO. C-UA-DL11-0-0	SIZE A	CODE PL	NUMBER DL11-0-0	REV. D	ECO NO. DL11-00006
	SHEET 1 OF 1	DIST. G				

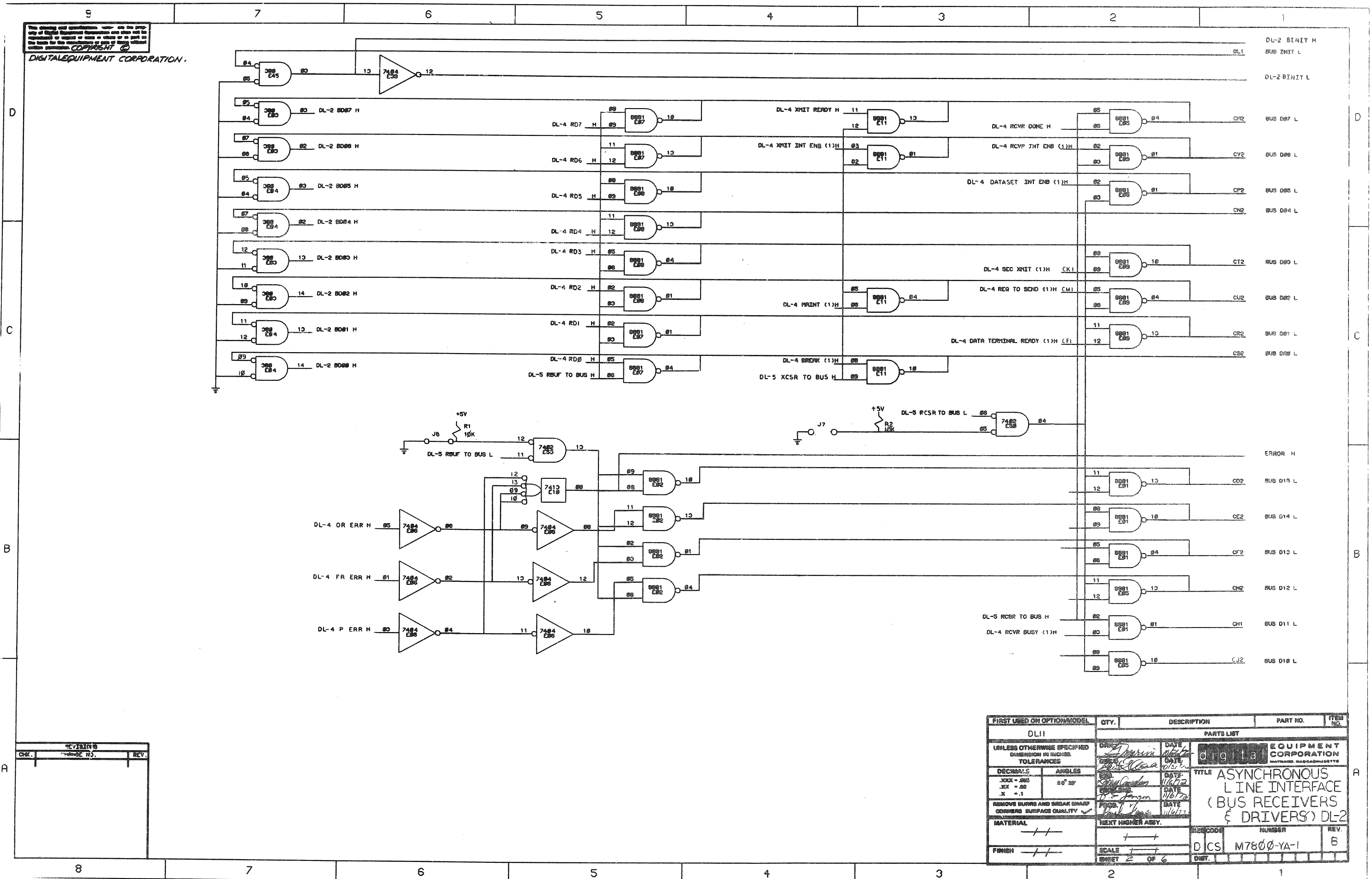


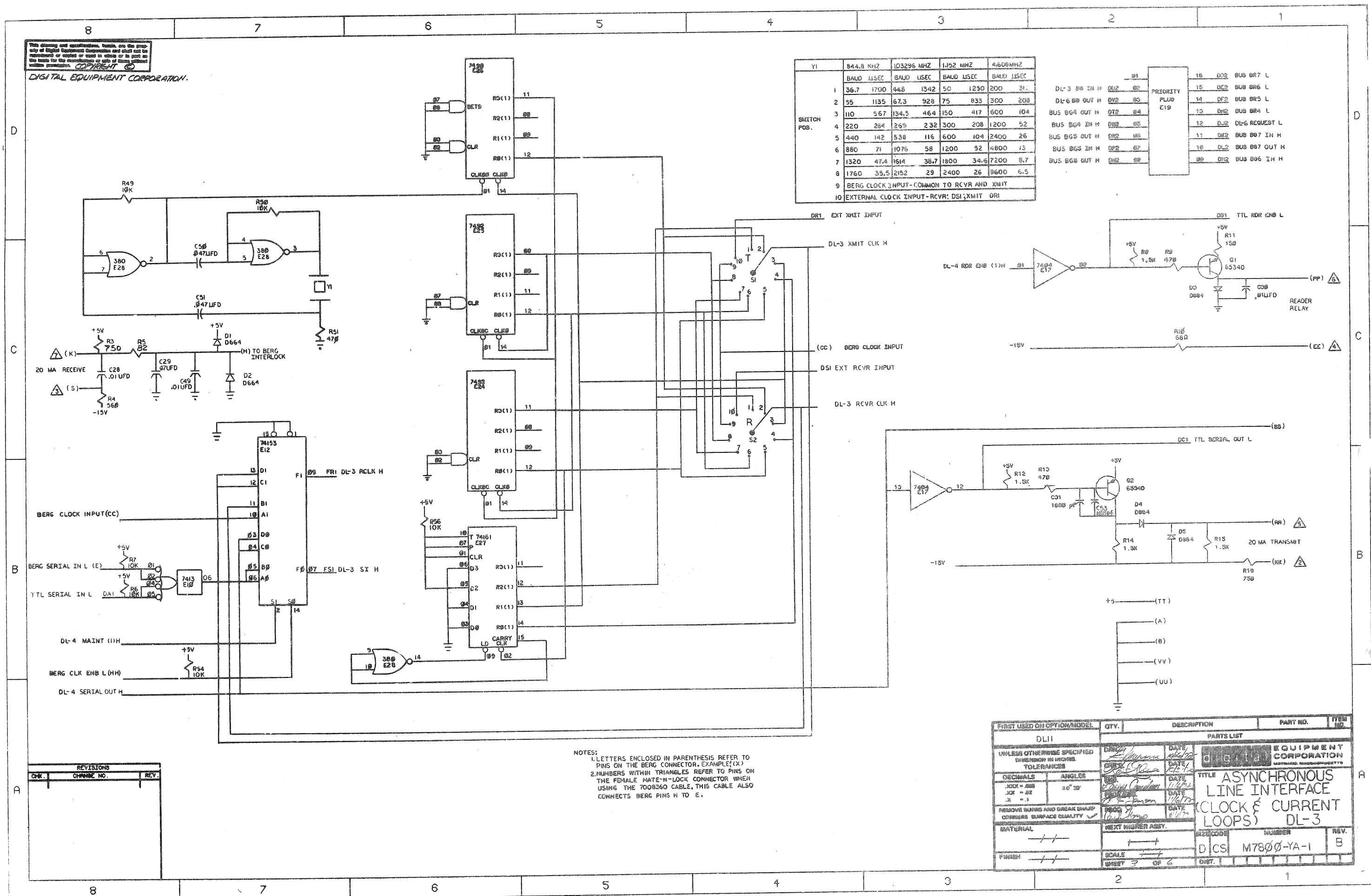
ALLOWABLE SUBSTITUTION LIST			
ORIG.	SUBSTITUTE	PART	ITEM
PART NO.	DESCRIPTION	PART NO.	NO.
1909489	IC 11380	1911115	23

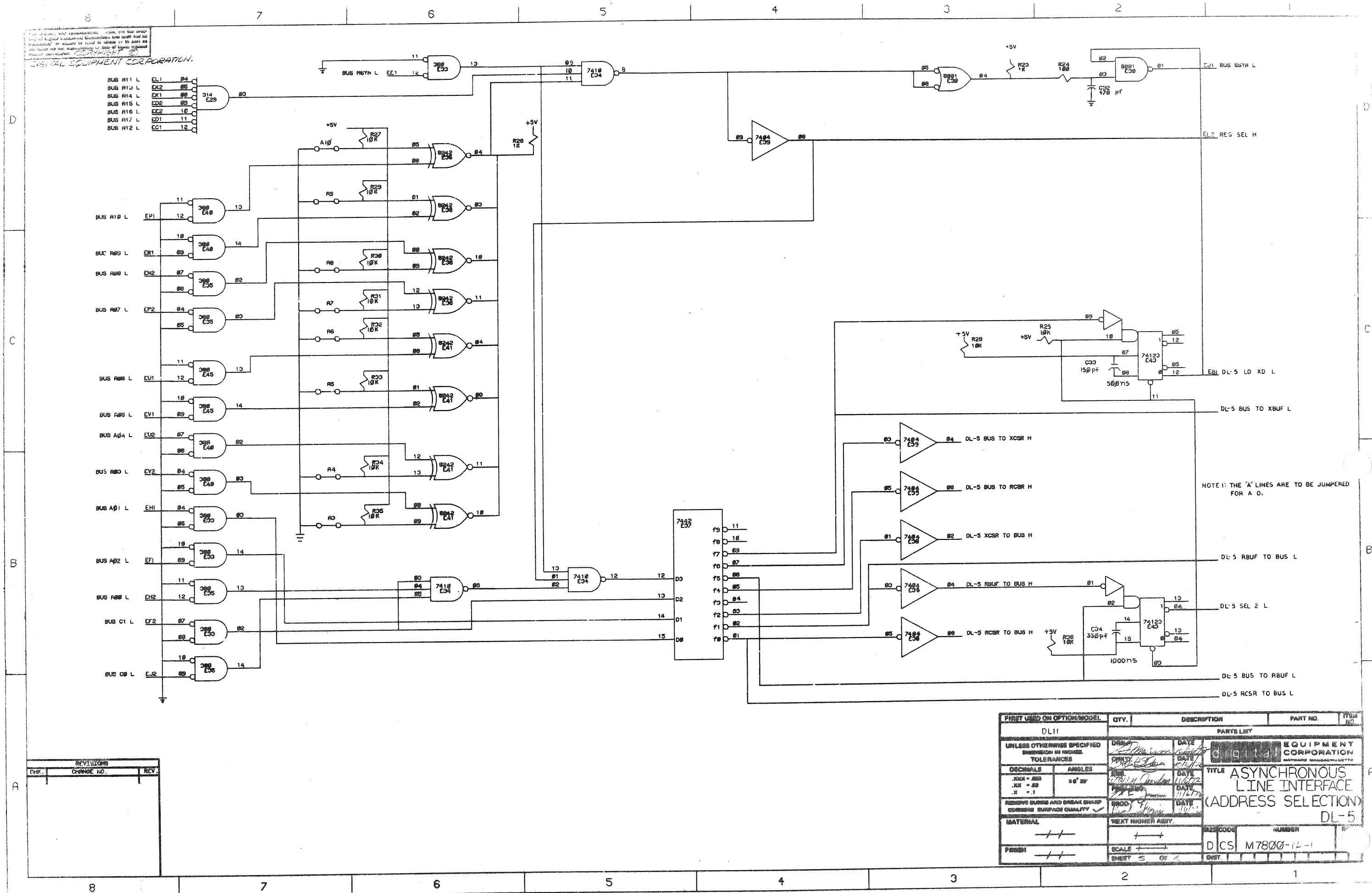
QTY	REP DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	R3	RES 750J 1/4W 5%	1301401	67
1	R3B	RES 390 1/4W 5%	1300309	68
1	D6	DIODE 1N742A	1100430	69
2	Q1, Q2	TRANSISTOR 6534A	13040100	70
1	R5	CAP 100P 100V 5% WAFER	10000006	63
1	C5	CAP 500P 100V 5% WAFER	10000025	64
2	R20, C51	CAP .047M CERALAM	10006678	61
1	E27	IC DEC 74161	13010650	60
2	C54, C55	0.00330F 100V 5% DIFFER MICH	10000213	59
1	C31	CAP 970P 100V 5% DIFFER MICH	10000629	58
1	E27	IC DEC 74001 5% DIFFER MICH	10000012	57
24	R1, R2, C3, C4, C5, C6, C7	0.001 100V 5% DIFFER MICH	10000010	56
1	R22	CAP .47UF 35V 10% TANT	10005945	55
3	R21 - 20K, C32, C37	CAP .68UF 35V 20% TANT	10000067	54
1	C33	CAP 1500P 100V 5% DIFFER MICH	10000017	53
2	R14, R15	RES 1.5K 1/4W 5%	13001594	52
5	R23, R5, R6	RES 470 1/4W 5%	1300165	51
1	R17	RES 68 1/4W 5%	13000205	50
1	R18	RES 68 1/4W 5%	1300220	49
1	R5	RES 68 1/4W 5%	1301477	48
1	R24	RES 100 1/4W 5%	1300329	47
1	R7	RES 150 1/4W 5%	13000507	46
1	R22	RES 150 1/4W 5%	1300352	45
1	R25	RES 200 1/4W 5%	1300371	44
2	R1 - R5	DIODE 1N4001 201 100MA	11001114	43
1	R5, R13, R51	RES 470 1/4W 5%	1300336	42
1	R4	RES 500 1/4W 5%	1300338	41
1	R1	WIRE 16X .125	50000255	40
1	R16	RES 500 1/4W 5%	1302385	39
26	R1, R2, R6, R7, R17, R19 - R20, R25, R27 - R33, R37, R47, R50, R52, R53, R56	RES 10K 1/4W 5%	1300477	38
1	R60, R12	RES 1.5K 1/4W 5%	1300391	37
1	E23	IC DEC 74001	1300334	36
1	E32, E33, E51, E62	IC DEC 74174	1300547	35
2	E36, E41	IC DEC 6242	1300712	34
3	E37, E39, E39	IC DEC 7408	13010135	33
2	E20, E25	SCAP 8PH 16 PIN *2.56X.256	50006001-1	32
1	E26, E27	IC DEC 7480	1300005	31
1	E16, E17, E67 - E71, E74, E30, E31, E34, E36	IC DEC 8981	1300725	30
2	E1	ALIST 8000 RG-1	1202212	29
1	E43	IC DEC 74123	1300236	28
3	E44, E45, E46	IC DEC 74174	1300567	27
2	E46, E50, E55	IC DEC 7400	1300703	26
1	E10	IC DEC 74174	1300589	25
2	E50, E53	IC DEC 7402	1300900	24
3	E54, E57, E58, E59, E60, E61, E66	IC DEC 380	13007483	23
1	E15	IC DEC 74153	1300957	22
1	E60	IC DEC 74104	1300927	21
1	E25	IC DEC 7400	1300703	20
4	E62, E74, E38, E39	IC DEC 7402	1300963	19
1	E34	IC DEC 7493	13009035	18
1	E34	IC DEC 7410	1300357	17
1	E39	IC DEC 314	1300704	16
1	E37	IC DEC 7462	1300647	15
1	E46	IC DEC 8237	1300645	14
2	E18, E19	IC DEC 74175	1300651	13
1	E14	RESISTOR CRYSTAL HOLDER	3302825	12
1	E14	RESISTOR CRYSTAL HOLDER	3303174	11
1	E14	IC SOCKET	1200895	10
2	S1, S2	SWITCH, SINGLE POLE, 10 POS	13000021	9
1	E1	NO PIN CONNECTOR BNC	1300011	8
1	E1	COIL 200K	9000135	7
1	E1	COIL 200K	9000285	6
1	E1	WAXIDE, 1/2-CHIP, MAGENTA	9000937-06	5
1	E1	ETCHED CIRCUIT BOARD	3000978	4
1	E1	WAXIDE 60 HISTORY	60000000-06	3
1	E1	ASSY/INSTALLING HOLE LAYOUT	60000000-05	2
1	E1	COIL COORDINATE HOLE	60000000-04	1

* SEE ALLOWABLE SUBSTITUTION
LIST & NOTE 4.

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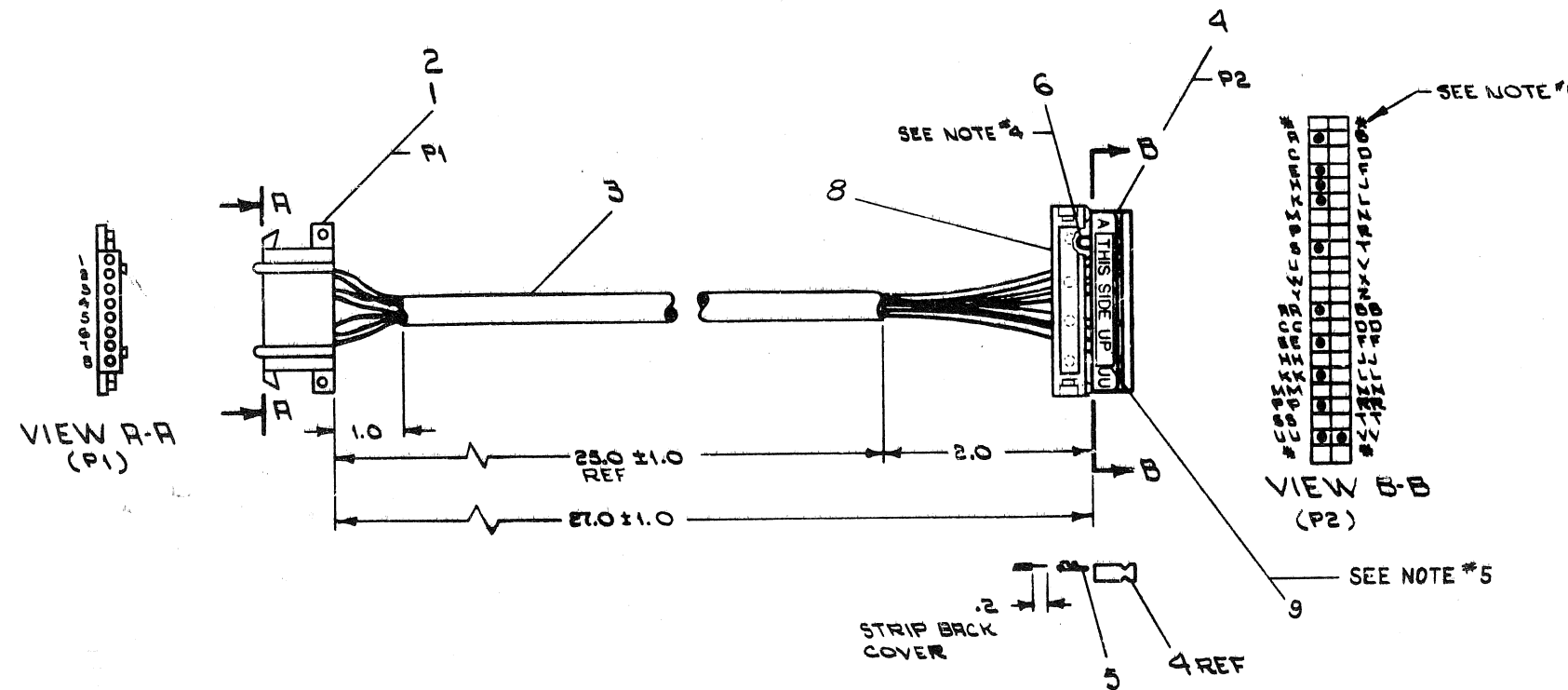
FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
DLII		PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES		DATE 1/16/72	DATE 1/16/72	DIGITAL EQUIPMENT CORPORATION ADDRESS 00000000000000000000	
TOLERANCES		DATE 1/16/72	DATE 1/16/72	TITLE ASYNCHRONOUS LINE INTERFACE	
DECIMALS	ANGLES	DATE 1/16/72	DATE 1/16/72	(ADDRESS SELECTION)	
.XXX - .000	30° 35'	DATE 1/16/72	DATE 1/16/72	DL-5	
.XX - .00		DATE 1/16/72	DATE 1/16/72		
.X - .1		DATE 1/16/72	DATE 1/16/72		
REWORK DURING AND BREAK SHARP CHISELS SURFACE QUALITY		DATE 1/16/72	DATE 1/16/72		
MATERIAL		TEXT WORKER ASSY.			
PUNCH		SCALE		SIZE CODE NUMBER	
		SHEET 5 OF 6		D CS M7800-12-1	

NOTES:

- * ASTERISKS INDICATE CAVITIES NOT USED OR DESIGNATED BY LETTERS.
- DRAIN WIRES TO BE CUT BACK TO OUTER INSULATION ON P1 END OF CABLE ONLY. SHIELDS TO BE CUT BACK TO OUTER INSULATION ON BOTH ENDS OF CABLES.
- DRAIN WIRES ON P2 END OF CABLE TO BE EACH ENCLOSED WITH ITEM #7 (TUBING) FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER P2 CONNECTOR.
- ITEM #6 (WIRE) TO BE APPROXIMATELY ONE (1) INCH LONG.
- PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #4 (BERG HOUSING) AS SHOWN.

WIRE TABLE

ITEM NO.	AWG	COLOR	PAIR NO.	FROM CONNECTION WITH	TO CONNECTION WITH
3	22	BLK	1	P1-2	2 P2-KK
3		RED	1	P1-3	2 P2-S
3,7		SHIELD		SEE NOTE #2	P2-R (NOTE #3)
3		BLK	2	P1-4	2 P2-EE
3		WHT	2	P1-5	2 P2-AA
3,7		SHIELD		SEE NOTE #2	P2-UK (NOTE #3)
3		BLK	3	P1-6	2 P2-PP
3		GRN	3	P1-7	2 P2-K
3,7		SHIELD		SEE NOTE #2	P2-V (NOTE #3)
6	22	BLK	-	P2-E	5 P2-H



QTY.	DESCRIPTION	PART NO.
1	LABEL, THIS SIDE UP	361567
1	STRAIN RELIEF	121166
1	RTUB. #18 TEF. THINWALL WRT	9101278-11
1	WIRE #22 AWG STRO TEF BLK	9101350-00
1	SOCKET, CRIMP #47216	1210089-07
1	HOUSING, BERG #65043-315	1210913-15
1	CABLE, BELDEN #3177-3PR SHLD	9101723-0
6	CONTACT MATE-LOCK (FEMALE)	1209379
1	CONN. MATE-LOCK (FEMALE)	1209340-00

FIRST USED ON OPTION/MODEL PDP-8E		DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES FINISH SURFACE QUALITY REMOVE BURRS AND BREAK SHARP EDGES		DATE 1/2/71 DATE 1/2/71 DATE 1/2/71 DATE 1/2/71 DATE 1/2/71		EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
MATERIAL SEE PARTS LIST		NEXT HIGHER ASSY A-ML-KLB-E-0		SCALE NONE		CABLE ASSEMBLY (KL8E)	
FINISH		SHEET 1 OF 1		DIST.		DIA 7008360-0-0	

REV.	CHANGE NO.	DATE	BY	CHK.
1	KL8E-00002	5/12/71	J. MCNEARA	
2	KL8E-00006	5/12/71	J. MCNEARA	
3	KL8E-00006	5/12/71	J. MCNEARA	
4	KL8E-00006	5/12/71	J. MCNEARA	
5	KL8E-00006	5/12/71	J. MCNEARA	
6	KL8E-00006	5/12/71	J. MCNEARA	
7	KL8E-00006	5/12/71	J. MCNEARA	
8	KL8E-00006	5/12/71	J. MCNEARA	
9	KL8E-00006	5/12/71	J. MCNEARA	
10	KL8E-00006	5/12/71	J. MCNEARA	
11	KL8E-00006	5/12/71	J. MCNEARA	
12	KL8E-00006	5/12/71	J. MCNEARA	
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80	KL8E-00006	5/12/71	J. MCNEARA	
81	KL8E-00006	5/12/71	J. MCNEARA	
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83	KL8E-00006	5/12/71	J. MCNEARA	
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85	KL8E-00006	5/12/71	J. MCNEARA	
86	KL8E-00006	5/12/71	J. MCNEARA	
87	KL8E-00006	5/12/71	J. MCNEARA	
88	KL8E-00006	5/12/71	J. MCNEARA	
89	KL8E-00006	5/12/71	J. MCNEARA	
90	KL8E-00006	5/12/71	J. MCNEARA	
91	KL8E-00006	5/12/71	J. MCNEARA	
92	KL8E-00006	5/12/71	J. MCNEARA	
93	KL8E-00006	5/12/71	J. MCNEARA	
94	KL8E-00006	5/12/71	J. MCNEARA	
95	KL8E-00006	5/12/71	J. MCNEARA	
96	KL8E-00006	5/12/71	J. MCNEARA	
97	KL8E-00006	5/12/71	J. MCNEARA	
98	KL8E-00006	5/12/71	J. MCNEARA	
99	KL8E-00006	5/12/71	J. MCNEARA	
100	KL8E-00006	5/12/71	J. MCNEARA	

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

SOFTWARE LIST

MADE BY ENPellegrini
DATE 8/29/72

ENG	P. Janson
DATE	8/29/72

CHECKED *3/1/72*
DATE *8-30-72*

PROD	<i>21420</i>
DATE	<i>8-31-72</i>

SECTION

ISSUED SECT.

LEGEND

D DOCUMENT
DN DOCUMENT CHANGE
NOTICE

PA	PAPER TAPE ASCII
PB	PAPER TAPE BINARY
PM	PAPER TAPE READ-IN-MODE

QUANTITY / VARIATION

[illegible]

DEC FORM NO. DEC 16 (327) 1049 N471
DPA 120

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS						
TITLE DL11 INSTALLATION PROCEDURE						
DATE 6-21-72						
REVISIONS						
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	CHANGE PER ECO	DL11-4	JANSON	3/73	P. Janson	4-6-73
D	CHANGE PER ECO	DL11-5	CONDON	7/73	P. Condon	8/6/73
ENG	PAUL E. Janson		APPD	Paul E. Janson		
DEC FORM NO. DRA 107A		SIZE	CODE	NUMBER	REV	
		A	SP	DL11-0-2	D	
SHEET 1 OF 8						

ENGINEERING SPECIFICATION			CONTINUATION SHEET		
TITLE DL11 INSTALLATION PROCEDURE					
DL11 INSTALLATION PROCEDURE:					
Installation of the M7800 module or its variation as a DL11-A through DL11-E option consists of the following preparations:					
1. Jumper insertion/deletion for selection of operation mode (A, B, C, D, or E).					
2. Register address assignment.					
3. Vector address assignment.					
4. Priority assignment.					
5. Special NPR jumper insertion/deletion.					
6. Selection of data format (data bits, stop bits, parity).					
7. Selection of crystal for baud rate.					
8. Installation of G8000 in systems where +15v is not available.					
9. Filter capacitor selection for high baud rate current-loop.					
A. OPERATION MODE:					
The following describes the jumpers associated with controlling the mode of operation (A,B,C,D, or E):					
J1. Ties EIA driver to REQUEST-TO-SEND lead (pin 4) of dataset cable. IN for DL11-B,D, and E; does not affect DL11-A and C. Drawing DL-7.					
J2. Ties EIA driver, normally used for the REQUEST-TO-SEND lead, to FORCE BUSY lead (pin 25) for use with Bell 103E. This is a customer option. If not specified, jumper is OUT for all DL11's. Drawing DL-7.					
J3. When inserted, allows REQUEST-TO-SEND lead (pin 4) to be controlled by bit 2 of the receiver status register. OUT for DL11-B and D; IN for DL11-E; does not affect DL11-A and C. Drawing DL-4.					
J4. When inserted, forces "DATA LEADS ONLY" mode of EIA operation. Turns DATA TERMINAL READY (pin 20) and REQUEST-TO-SEND (pin 4) on. IN for DL11-B and D; OUT for DL11-E; does not affect DL11-A and C. Drawing DL-4.					
J5. When inserted, allows the BREAK bit to function. OUT for DL11-A and B; IN for DL11-C,D, and E. Drawing DL-4.					
J6. When inserted, allows DSET INT to cause interrupts. OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-4.					
J7. When inserted, allows dataset control bits to be read as part of the receiver status register.					
DEC FORM NO. DRA 108		DEC 16-(381)-1022-N370	SIZE	CODE	NUMBER
			A	SP	DL11-0-2
SHEET 2 OF 8					

ENGINEERING SPECIFICATION			CONTINUATION SHEET																
TITLE DL11 INSTALLATION PROCEDURE																			
J7. (con't)																			
OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-2.																			
J8. When inserted, allows error bits to be read as part of the receiver data register. OUT for DL11-A and B; IN for DL11-C,D and E. Drawing DL-2.																			
J9. If mode control jumpers:																			
JUMPER A B C D E DRAWING																			
J1					DL-7														
J2	OUT	IN	IN	OUT	DL-7														
J3	OUT	OUT	OUT	IN	DL-4														
J4	OUT	IN	IN	OUT	DL-4														
J5	OUT	OUT	IN	IN	DL-4														
J6	OUT	OUT	OUT	IN	DL-4														
J7	OUT	OUT	OUT	IN	DL-2														
J8	OUT	OUT	IN	IN	DL-2														
* = don't care																			
B. REGISTER ADDRESS ASSIGNMENTS:																			
The DL11 can respond to addresses with the following format:																			
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
1	1	1	1	1	1	1	1	1	1	JUMPERS									
Selects 1 of 4 Registers																			
Byte Control																			
Bits 10 through 3 are controlled by jumpers A10 to A3. A jumper inserted indicates a zero.																			
For the DL11-A and B used as the console device, address 777560 is assigned. For additional units, assign 776XX0, where XX=50 for the first additional unit and XX=67 for the 16th unit.																			
For the DL11-C,D and E assign address 77XXX0, where XXX=561 for the first line, and XXX=617 for the 31st line. Assign all C's first, then D's, and then E's.																			
DEC FORM NO. DRA 108		DEC 16-(381)-1022-N370		SIZE	CODE	NUMBER	REV												
				A	SP	DL11-0-2	D												
SHEET 3 OF 8																			

ENGINEERING SPECIFICATION			CONTINUATION SHEET		
TITLE DL11 INSTALLATION PROCEDURE					
C. VECTOR ADDRESS ASSIGNMENT:					
Jumpers V8 through V3 control the interrupt vector. A jumper inserted provides a vector bit of one. Vectors can be produced in the form XX0 and XX4, where XX ranges from 00 to 77.					
For the DL11-A and B used as a console device the vector address is 060/064. For additional units, vectors are floating.					
For the DL11-C,D, and E, vector addresses are floating. Assign all C's first, then D's, then E's.					
D. PRIORITY ASSIGNMENT:					
Interrupt priority is established by inserting a "priority plug" in the socket at IC location E19. For DL11-A,B,C,D and E use level 4.					
SUMMARY OF REGISTER, VECTOR AND PRIORITY ASSIGNMENTS:					
		ADDRESS	VECTOR	PRIORITY	
DL11-A,B CONSOLE		777560			
		777562	60/64	BR4	
		777564			
		777566			
DL11-A,B ADDITIONAL UNITS		776XX0	Floating	BR4	
		776XX2			
		776XX4			
		776XX6			
	Where XX= 50 for line #1 and XX= 67 for line #16	ADDRESS	VECTOR	PRIORITY	
		77XXX0			
		77XXX2	Floating	4	
		77XXX4			
		77XXX6			
DL11-C,D,E		77XXX0			
		77XXX2			
		77XXX4			
		77XXX6			
	Where XXX= 561 for line #1 and XXX= 617 for line #31	ADDRESS	VECTOR	PRIORITY	
		77XXX0			
		77XXX2	Floating	4	
		77XXX4			
		77XXX6			
DEC FORM NO. DRA 108		DEC 16-(381)-1022-N370		SIZE	CODE
				A	SP
NUMBER DL11-0-2					
REV D					
SHEET 4 OF 8					

ENGINEERING SPECIFICATION		CONTINUATION SHEET																										
TITLE DL11 INSTALLATION PROCEDURE																												
E. SPECIAL NPR JUMPER: Jumper N1, shown on drawing DL-6, controls the response of the interrupt circuit to an NPR request. The jumper should normally be IN, except for 11/20 and 11/15 systems without the KHI1 option.																												
F. SELECTION OF DATA FORMAT:																												
1. Data Bits Split lug pairs NB2 and NB1 control the number of data bits in the serial character as follows:																												
<table><thead><tr><th>NB2</th><th>NB1</th><th># OF DATA BITS</th></tr></thead><tbody><tr><td>OUT</td><td>OUT</td><td>8</td></tr><tr><td>OUT</td><td>IN</td><td>7</td></tr><tr><td>IN</td><td>OUT</td><td>6</td></tr><tr><td>IN</td><td>IN</td><td>5</td></tr></tbody></table>				NB2	NB1	# OF DATA BITS	OUT	OUT	8	OUT	IN	7	IN	OUT	6	IN	IN	5										
NB2	NB1	# OF DATA BITS																										
OUT	OUT	8																										
OUT	IN	7																										
IN	OUT	6																										
IN	IN	5																										
2. Parity Parity is controlled by split lug pairs NP and EPS as follows:																												
<table><thead><tr><th>NP</th><th>EPS</th><th>PARITY</th></tr></thead><tbody><tr><td>OUT</td><td>OUT</td><td>OFF</td></tr><tr><td>OUT</td><td>IN</td><td>OFF</td></tr><tr><td>IN</td><td>OUT</td><td>EVEN</td></tr><tr><td>IN</td><td>IN</td><td>ODD</td></tr></tbody></table>				NP	EPS	PARITY	OUT	OUT	OFF	OUT	IN	OFF	IN	OUT	EVEN	IN	IN	ODD										
NP	EPS	PARITY																										
OUT	OUT	OFF																										
OUT	IN	OFF																										
IN	OUT	EVEN																										
IN	IN	ODD																										
3. Stop Bits Split lug pair 2SB and jumpers J9, J10 and J11 control the number of stop bits in the serial character as follows:																												
<table><thead><tr><th>2SB</th><th>J9</th><th>J10</th><th>J11</th><th># OF STOP BITS</th></tr></thead><tbody><tr><td>OUT</td><td>OUT</td><td>IN</td><td>OUT</td><td>2</td></tr><tr><td>IN</td><td>OUT</td><td>IN</td><td>OUT</td><td>1</td></tr><tr><td>IN</td><td>OUT</td><td>OUT</td><td>IN</td><td>1.5 for TI, GI, and SCM UARTS</td></tr><tr><td>IN</td><td>IN</td><td>OUT</td><td>OUT</td><td>1.5 for WD UARTS</td></tr></tbody></table>				2SB	J9	J10	J11	# OF STOP BITS	OUT	OUT	IN	OUT	2	IN	OUT	IN	OUT	1	IN	OUT	OUT	IN	1.5 for TI, GI, and SCM UARTS	IN	IN	OUT	OUT	1.5 for WD UARTS
2SB	J9	J10	J11	# OF STOP BITS																								
OUT	OUT	IN	OUT	2																								
IN	OUT	IN	OUT	1																								
IN	OUT	OUT	IN	1.5 for TI, GI, and SCM UARTS																								
IN	IN	OUT	OUT	1.5 for WD UARTS																								
G. CRYSTAL SELECTION: The clocking scheme of the DL11 consists of a single crystal oscillator feeding a divider network, with two 10-position switches tapping various points to feed into the UART's																												

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D
SHEET 5		OF 8	

DEC FORM NO DEC 16-(381)-1022-4370
DRA 108

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DL11 INSTALLATION PROCEDURE			
H. G8000 INSTALLATION: For DL11-B, D, and E a positive voltage is required between 9 and 15 volts to operate the EIA drivers. For PDP-11/20 and PDP-11/15 systems with the M720 power supply, a G8000 module must be installed to provide this voltage. Using a filter network, this module converts the full-wave rectified "+8V" signal to a positive DC voltage. 1. Install G8000 into slot AP2 of DD11-A. 2. Wire AP3V2 to AP2V2. 3. Wire AP2M2 to CXXU1 where XX is the slot location of the M7800. Refer to diagram 1.			
I. FILTER CAPACITOR SELECTION: For DL11-A's and DL11-C's, which operate with 20ma current loops capacitors are used to filter the receive line and slow the switching time of the transmit line. To avoid excessive distortion above 150 baud, the capacitance in each of these two circuits must be reduced. This is accomplished by clipping C29 (.47 mfd) and C31 (1000 pf), both shown on drawing DL-3. J. DL11-B, D, E in Systems with +15V available using DD11-A There is a special situation of using a DD11-A to mount a DL11-B, D, Or E in systems with +15V available. These systems have +15V available and it appears at pin AP3V2 of the DD11-A when using power harness such as 7009177, 7008955, or 7008909. In this situation, no G8000 is necessary, and +15V can be wired directly from AP3V2 to CXXU1, where XX is the slot number of the DL11. NOTE: this does not apply to DL11-A or C or DD11-B. K. When using the DL11-B, D, E in an 11/05 processor pin CXXU1 has +15V available on it so no G8000 or no jumpers are required.			

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D
SHEET 7		OF 8	

DEC FORM NO DEC 16-(381)-1022-4370
DRA 108

ENGINEERING SPECIFICATION		CONTINUATION SHEET																																																																	
TITLE DL11 INSTALLATION PROCEDURE																																																																			
G. Con't transmitter and receiver sections. Thus, for a given crystal frequency, 8 baud rates are independently selectable for transmit and receive. The two addition switch positions select external clocks.																																																																			
<table><thead><tr><th>SPEED GROUP</th><th>1</th><th>2</th><th>3</th><th>4</th></tr></thead><tbody><tr><td colspan="5">CRYSTAL (KHZ)</td></tr><tr><td>POSITION</td><td>FACTOR</td><td>844.8K</td><td>1.03296M</td><td>1.152M</td><td>4.608M</td></tr><tr><td>1*</td><td>23040</td><td>36.7</td><td>44.8</td><td>50</td><td>200</td></tr><tr><td>2</td><td>15360</td><td>55</td><td>67.3</td><td>75</td><td>300</td></tr><tr><td>3</td><td>7680</td><td>110</td><td>134.5</td><td>150</td><td>600</td></tr><tr><td>4</td><td>3840</td><td>220</td><td>269</td><td>300</td><td>1200</td></tr><tr><td>5</td><td>1920</td><td>440</td><td>538</td><td>600</td><td>2400</td></tr><tr><td>6</td><td>960</td><td>880</td><td>1076</td><td>1200</td><td>4800</td></tr><tr><td>7</td><td>640</td><td>1320</td><td>1614</td><td>1800</td><td>7200</td></tr><tr><td>8</td><td>480</td><td>1760</td><td>2152</td><td>2400</td><td>9600</td></tr></tbody></table>				SPEED GROUP	1	2	3	4	CRYSTAL (KHZ)					POSITION	FACTOR	844.8K	1.03296M	1.152M	4.608M	1*	23040	36.7	44.8	50	200	2	15360	55	67.3	75	300	3	7680	110	134.5	150	600	4	3840	220	269	300	1200	5	1920	440	538	600	2400	6	960	880	1076	1200	4800	7	640	1320	1614	1800	7200	8	480	1760	2152	2400	9600
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8	480	1760	2152	2400	9600																																																														
Most counter-clock wise position. To determine a crystal frequency for a non-standard baud rate, pick the position of the closest baud rate in the 1.152MHz column, and then multiply the non-standard baud rate by the factor for that position. For example, if the customer specifies 1050 baud, this is closest to 1200 baud, position 6. 1050 X 960 = 10080000 = 1.008MHZ. The crystal frequency should not fall outside the range of the standard crystals. DEC part numbers for the standard crystals are as follows: 844.8 KHZ 18-10245-1 1.03296 MHZ 18-05501-6 1.152 MHZ 18-05501-5 4.608 MHZ 18-05501-7 *Use A or C cut crystals only. Do not use crystals marked NE-6D. When ordering a special crystal, refer to purchase specification 18-05501 for crystal specification. Insure that transparent vinyl tape (9008269) is applied to the top surfaces of the crystal and mounting brackets to insulate from adjacent modules.																																																																			

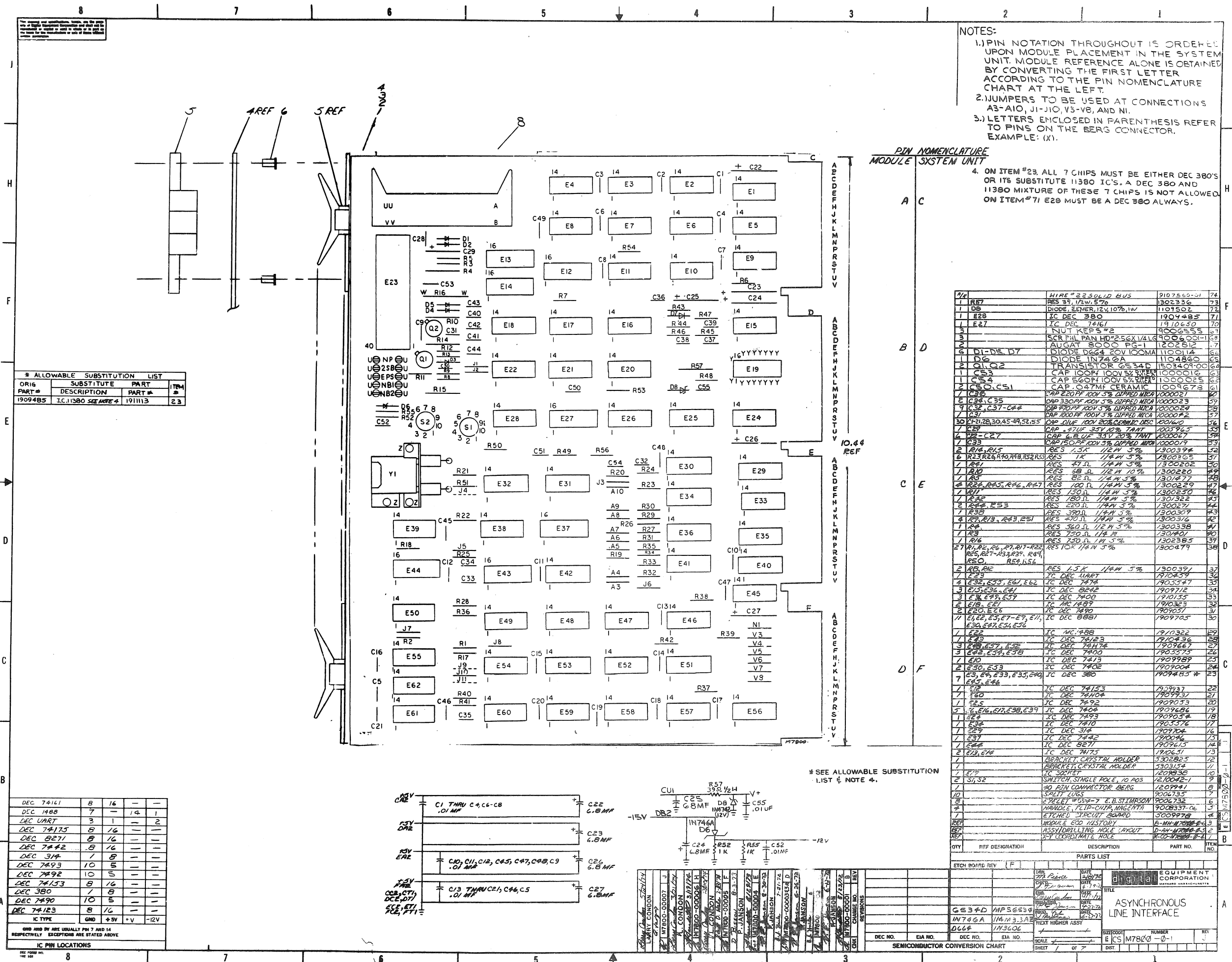
SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D
SHEET 6		OF 8	

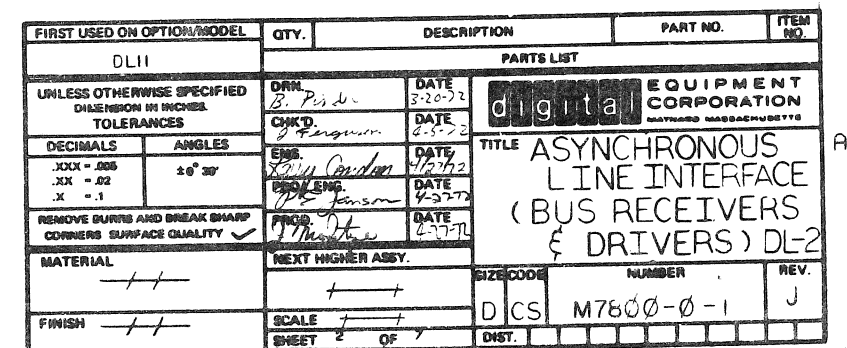
DEC FORM NO DEC 16-(381)-1022-4370
DRA 108

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DL11 INSTALLATION PROCEDURE			
DIAGRAM 1. G8000 INSTALLATION Diagram 1: G8000 INSTALLATION. The diagram shows a G8000 module connected to a FILTER NETWORK and a POWER CONNECTOR. The G8000 module has pins M7300, N2, and V2. The FILTER NETWORK has pins N2 and V2. The POWER CONNECTOR has pins V2 and A03. The connections are: M7300 to N2, N2 to V2, and V2 to A03.			

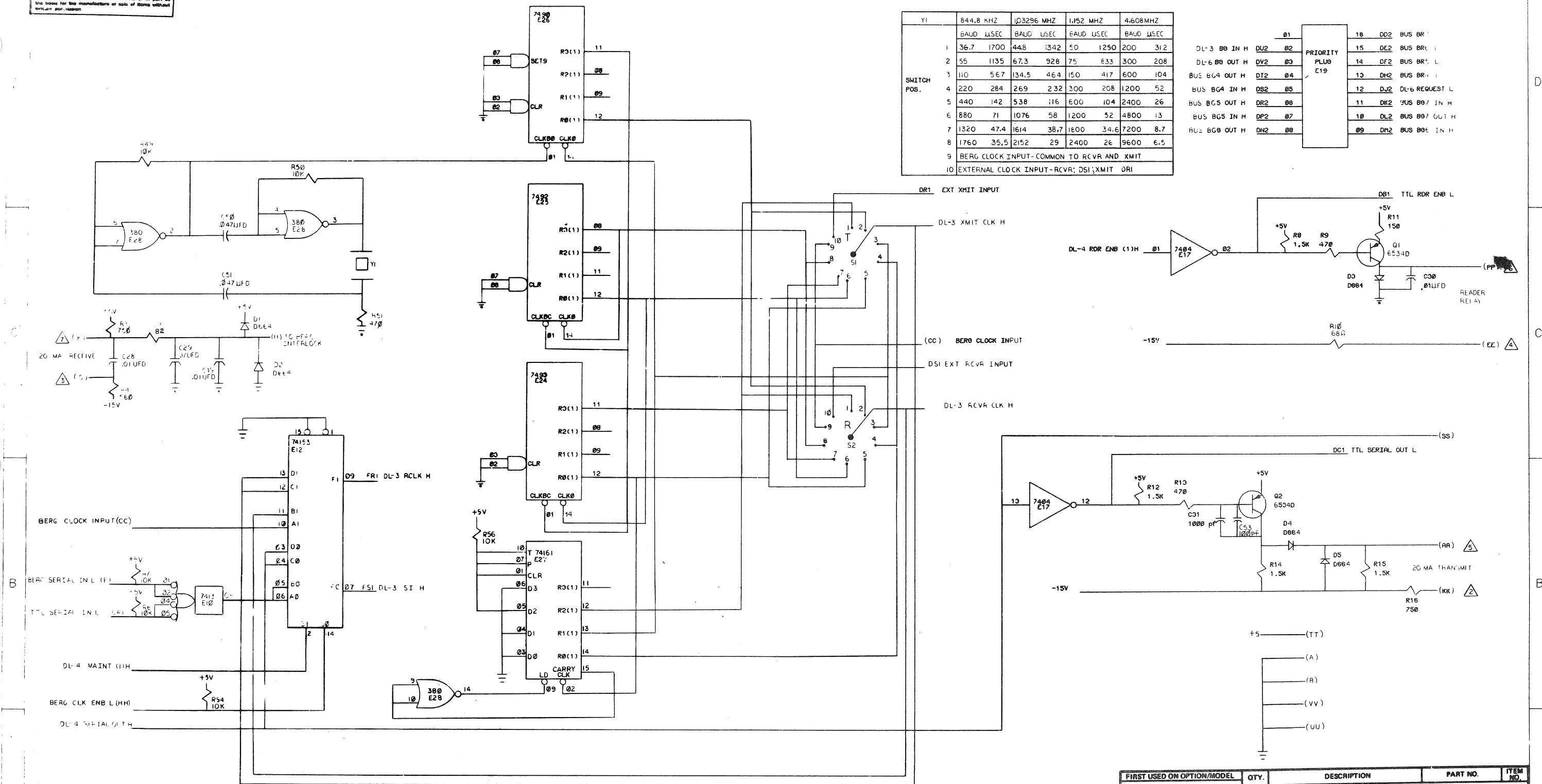
SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D
SHEET 8		OF 8	

DEC FORM NO DEC 16-(381)-1022-4370
DRA 108





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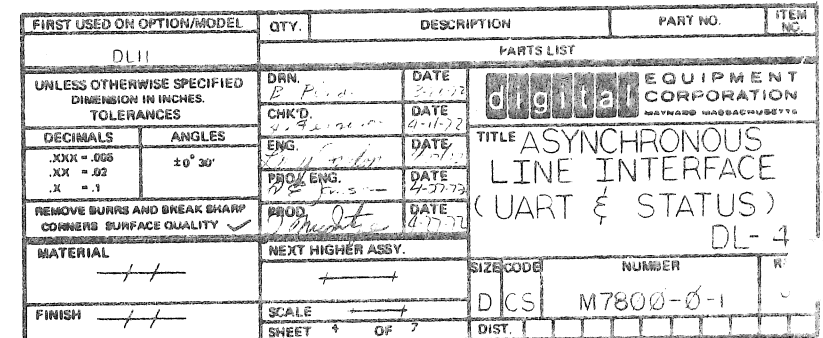


NOTES:

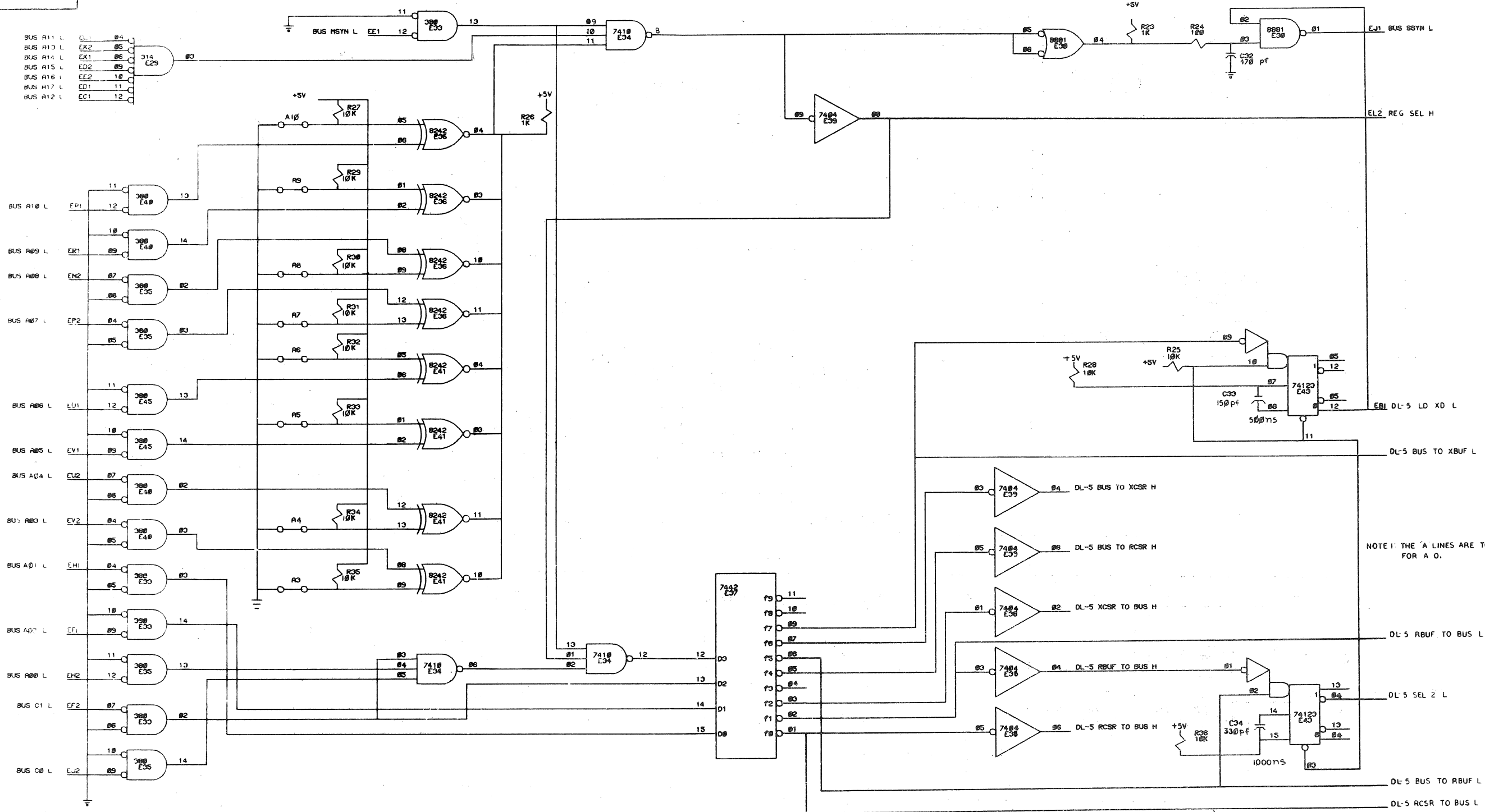
- 1.LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE;(X)
- 2.NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE 700B360 CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
DLII			PARTS LIST		
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES. TOLERANCES		DRAWN <i>B. Ford</i>	DATE 3-20-72	 DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
		CHECKED <i>J. Ford</i>	DATE 4-5-72		
DECIMALS	ANGLES	ENG. <i>Sam Gordon</i>	DATE 4/2/72	TITLE ASYNCHRONOUS LINE INTERFACE (CLOCK & CURRENT LOOPS) DL-3	
.XXX = .008	20° 30'	PROD. ENG. <i>P. Jensen</i>	DATE 4-27-72		
.XX = .02		PROD. DES. <i>J. M. Dwyer</i>	DATE 4-17-72		
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓					
MATERIAL	NEXT HIGHER ASSY.		SIZE CODE	NUMBER	REV.
<i>++</i>	<i>++</i>		D/C S	M78000-0-1	J
FINISH	SCALE <i>++</i>		DIST.		
<i>++</i>	SHEET 3 OF 7				

[illegible]

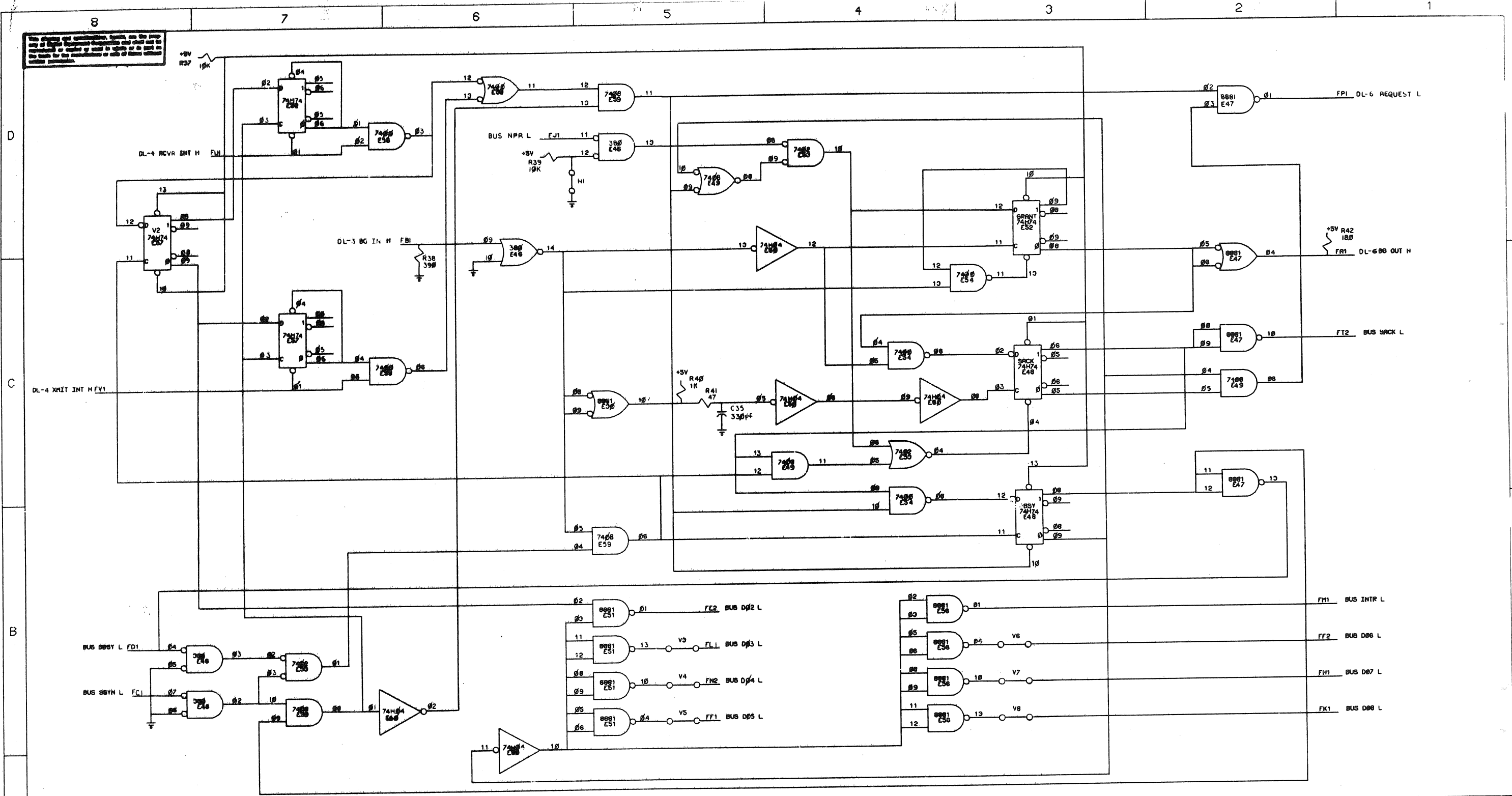
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NOTE 1: THE 'A' LINES ARE TO BE JUMPERED FOR A.O.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DL-5				
PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES		DRN 8. Powder	DATE 3-20-72	digital EQUIPMENT CORPORATION MILWAUKEE, WISCONSIN 53201
		CHK'D C. Ferguson	DATE 4-6-72	
DECIMALS	ANGLES	ENG. D. G. Gordon	DATE 4/21/72	
.XXX - .001	±0° 30'	PROD. ENG. C. Ferguson	DATE 5-27-72	
.XX - .01		PROD. M. B. B.	DATE 5-27-72	
.X - .1				
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓				
MATERIAL		NEXT HIGHER ASSY.		
++		++		
FINISH		SCALE		
++		SHEET 5 OF 7		
TITLE A SYNCHRONOUS LINE INTERFACE (ADDRESS SELECTION) DL-5				
REV. J				
D CS M7800-0-1				
DIST.				



NOTE: THE 'V' LINES ARE TO BE JUMPED FOR A I.

REVISIONS		
CHK.	CHNGE NO.	REV.

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
DLII					
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES.		PARTS LIST			
TOLERANCES		DRN	DATE	EQUIPMENT CORPORATION	
DECIMALS		CHK'D	DATE		
.XXX - .005	ANGLES	ENG.	DATE	TITLE ASYNCHRONOUS LINE INTERFACE (INTERRUPT CONTROL) DL-6	
.XX - .02	20' 30'	PROV. ENG.	DATE		
.X - .1		PROD. ENG.	DATE	NUMBER	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY		PROD. MGR.	DATE		
MATERIAL		NEXT HIGHER ASSY.		D CS M7800-0-1	
FINISH		SCALE		SHEET OF	
				DIST.	

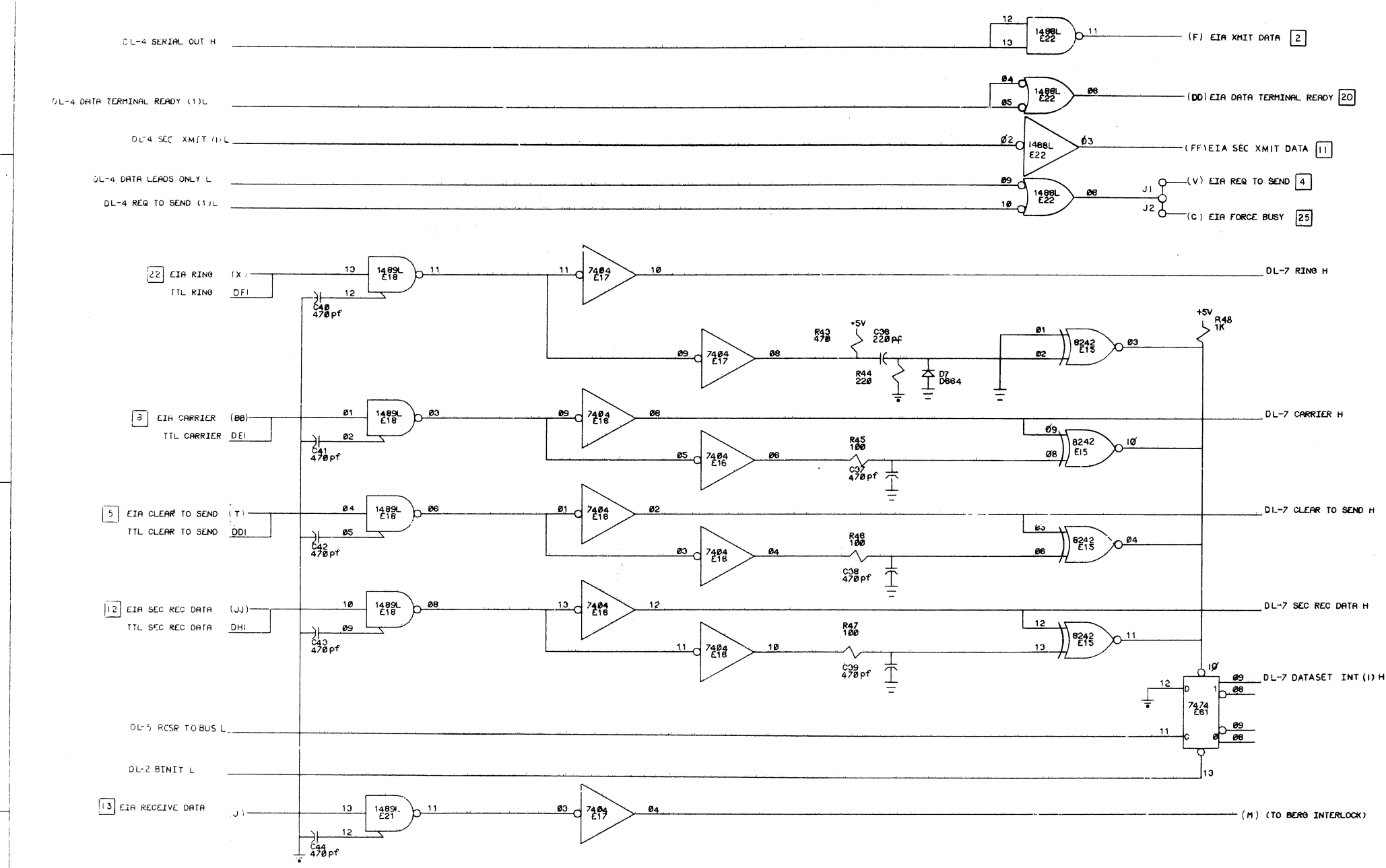
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D

C

B

A



- NOTES:
1. LETTERS ENCLOSED-EXAMPLE (M) REFER TO PINS ON THE BERG CONNECTOR.
 2. NUMBERS WITHIN BOXES REFER TO PINS ON THE MALE CINCH CONNECTOR WHEN USING THE BC05-C CABLE, THIS CABLE ALSO CONNECTS BERG PINS M TO E.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DLII				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	DRN B. P. P. 1	DATE 5-27-72	PARTS LIST	
DECIMALS	CHK'D D. G. 2-10-72	DATE 4-5-72	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
ANGLES	ENG R. W. J. Condon	DATE 4-5-72	TITLE ASYNCHRONOUS LINE INTERFACE (EIA DRIVERS & RECEIVERS) DL-7	
XXX - .005 .XX - .02 .X - .1	PROV'G D. G. 2-10-72	DATE 4-27-72		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	PROD M. J. 4-27-72	DATE 4-27-72		
MATERIAL	NEXT HIGHER ASSY.	SIZE CODE	NUMBER	REV
FINISH	SCALE	D CS	M7800-0-1	J
	SHEET 7 OF 7	DIST.		

8

7

6

5

4

3

2

1

0-0-09008

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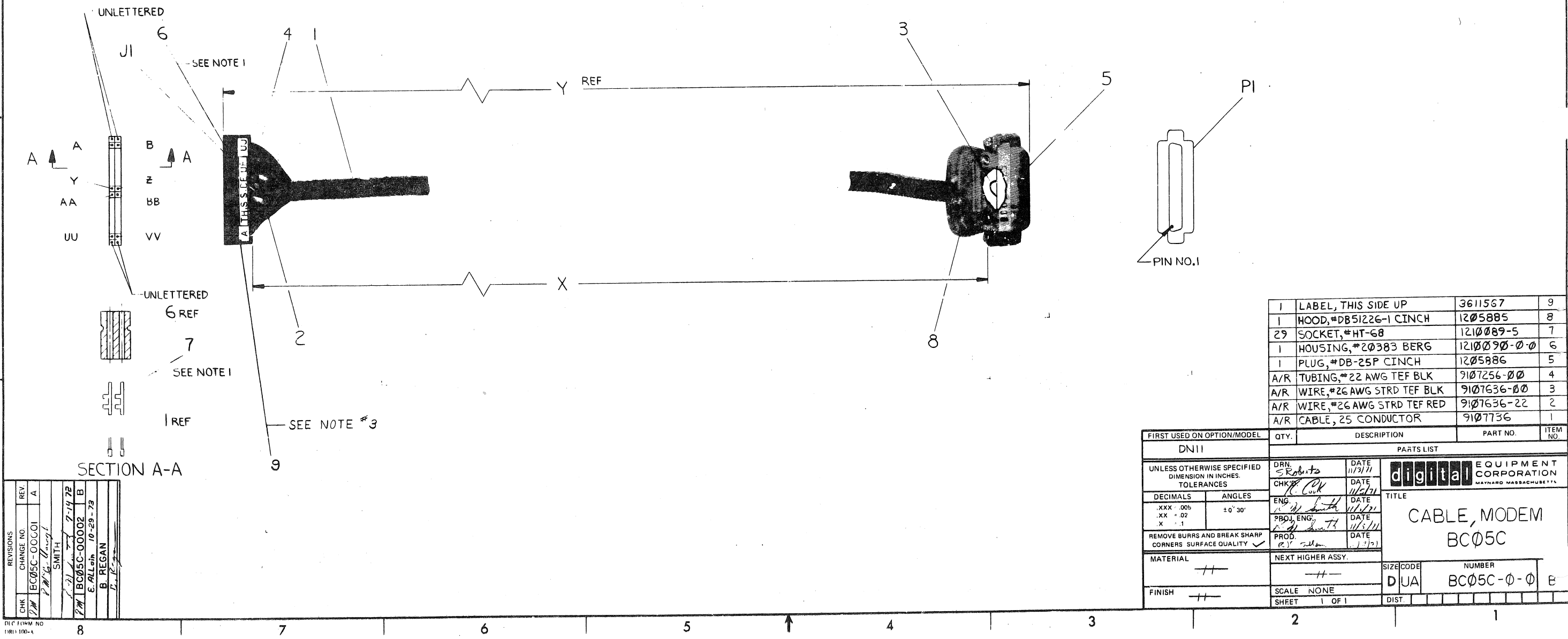
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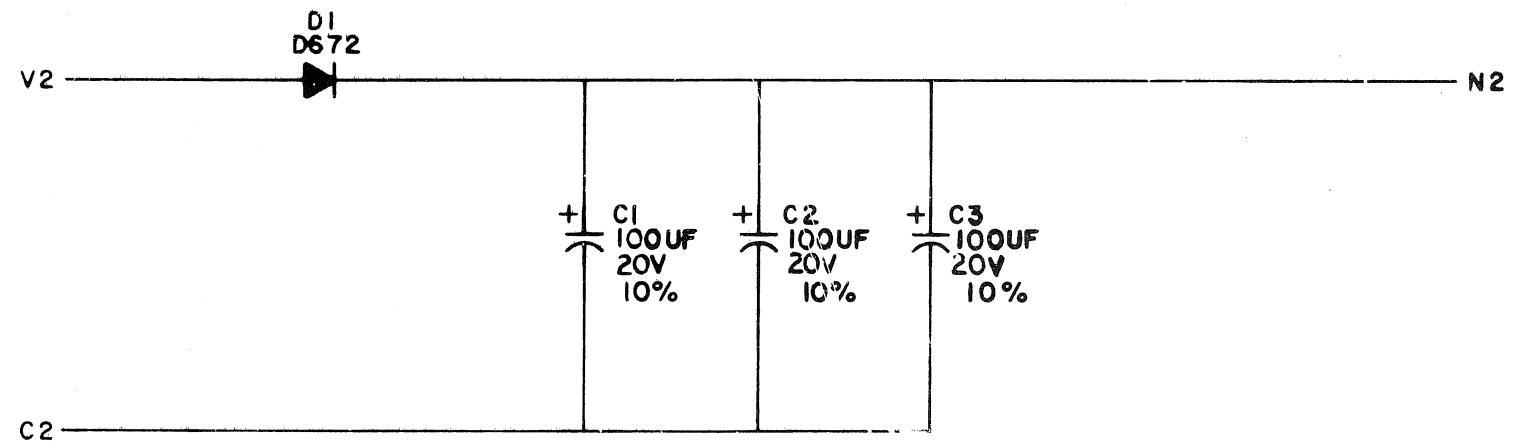
WIRE TABLE											
FROM			TO			FROM			TO		
ITEM NO.	AWG	COLOR	CONNECTION	WITH	CONNECTION	WITH	ITEM NO.	AWG	COLOR	CONNECTION	WITH
1	22	BLU/WHT	PI-1		JI-VV		1	22	RED/BRN	PI-16	
		WHT/BLU	PI-2		JI-F				SLA	PI-17	
		ORN/WHT	PI-3		JI-J				RED/SLA	PI-18	
		WHT/ORN	PI-4		JI-V				BLU/BLK	PI-19	
		GRN/WHT	PI-5		JI-T				BLK/BLU	PI-20	
		WHT/GRN	PI-6		JI-Z				ORN/BLK	PI-21	
		BRN/WHT	PI-7		JI-UU				BLK/ORN	PI-22	
		WHT/BRN	PI-8		JI-BB				GRN/BLK	PI-23	
		SLA/WHT	PI-9		JI-Y				BRN/RED	PI-24	
		WHT/SLA	PI-10		JI-W				RED/ORN	PI-25	
		BLU/RED	PI-11		JI-FF		1	22	BLK	PI-1	4
		RED/BLU	PI-12		JI-JJ		3	26	BLK	PI-1	4
		ORN/RED	PI-13		JI-D		2	26	RED	JI-E	
		SLA/RED	PI-14		JI-LL						
1	22	SLA/GRN	PI-15		JI-N						

LEGEND		
NUMBER	VARIATION	
	DIM X	DIM Y (PRE CUT)
BC05C-25	25'±3"	25'±1.8"
BC05C-50	50'±2%	50'±1.8"

- NOTES:
- MANUFACTURING SHOULD USE MACHINE CRIMPER TOOL FOR CRIMPING PINS (ITEM #7) MUST BE HT68 FROM BERG ELECT
 - ONLY DEC PART #1210090-0-0 MAY BE USED AS JI.
 - PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #6 (BERG HOUSING) AS SHOWN.



ALL INFORMATION IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE
CIRCUIT IS PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
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REVISIONS CHK'D NO. REV. L. J. JONES S. SHANNON J. J. JONES	DRN. S. COOPER	DATE 1/19/71	TRANSISTOR & DIODE CONVERSION CHART				digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	TITLE FILTER NETWORK G8000			
	CHK'D J. J. JONES	DATE 2/13/71	DEC	EIA	DEC	EIA		SIZE B	CODE CS	NUMBER G8000-0-1	REV. A
	ENG. R. S. JONES	DATE 3/11/71									
	PROD.	DATE									

DPC FORM NO
DBB 102

DIST. 324, 434, 435 2
4 PINK

D

C

B

A

H1		K24	EXTERNAL CLOCK
H2		K15	TRANSMIT CLOCK
J2		K17	RECEIVE CLOCK
E2		K2	TRANSMIT DATA
F2		K3	RECEIVE DATA
N2		K6	DATA SET READY
E1		K11	SECONDARY TRANSMIT DATA
F1		K12	SECONDARY RECEIVE DATA
R2		K20	DATA TERMINAL READY
P2		K5	CARRIER DETECT
K2		K5	CLEAR TO SEND
L2		K4	REQUEST TO SEND
S1		K25	FORCE BUSY
M2		K22	RING

CHOP
HERE

7		EXPLET FRED THRU	9006731	
1	J1	CNN. C1NCH DB-255-3	1210247	
1		ETCHED CIRCUIT BOARD	5010770	4
		MCUPL ECO HISTORY	A-NH-H315-0-6	3
		ASSY/DRILLING HOLE LAYOUT	C-AH-H315-0-5	2
		X- COORDINATE HOLE LOCATION	K-CO-H315-0-4	1
QTY.	REF. DESIGNATION	DESCRIPTION	OSC PART NO.	REP. NO.
		PA. PS. LIST		

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
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Q11	REF DESIGN	PARTS LIST
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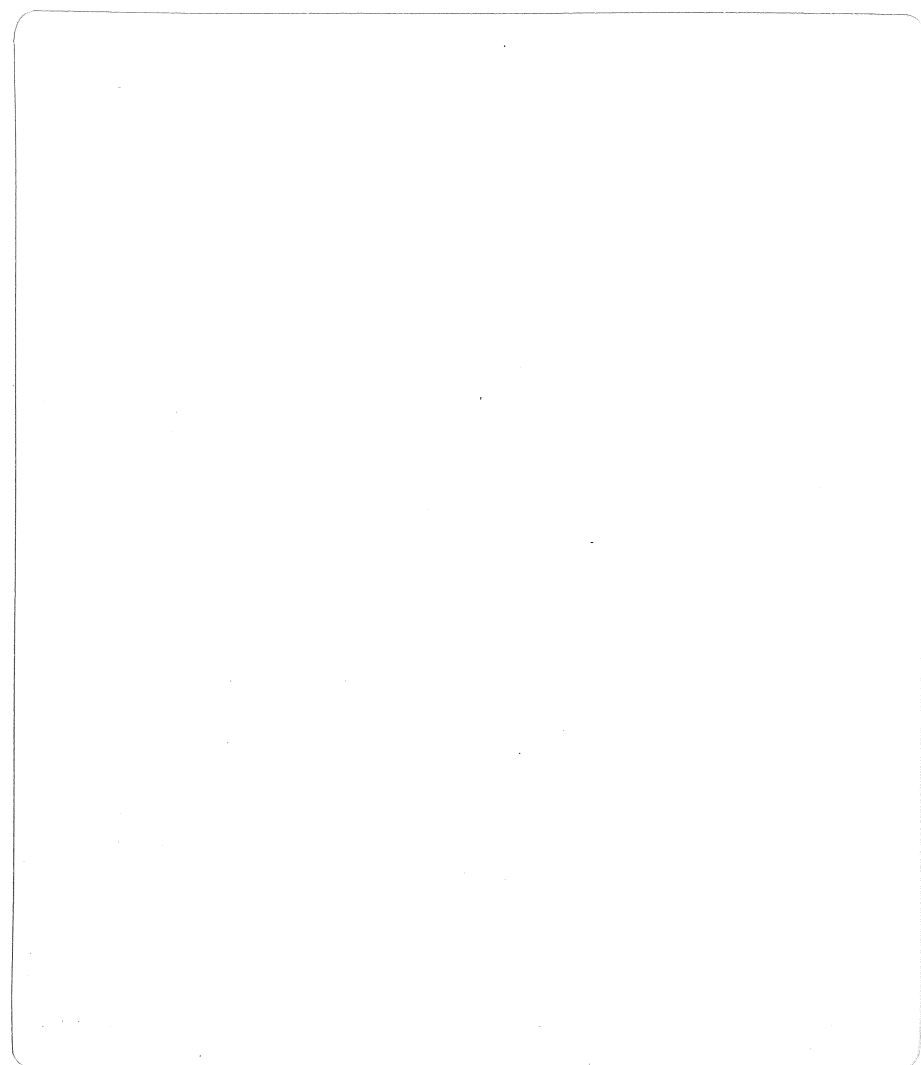
[illegible]

EXP. DATE	DRN <i>Kemper</i>	DATE	3-5-72	 EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
	CHAD. <i>Harrell</i>	DATE	3-8-72	
	ENG. <i>W. S. G. Smith</i>	DATE	3-12-72	
	PROD. ENG. <i>W. S. G. Smith</i>	DATE	3-13-72	
	PROD. <i>W. S. G. Smith</i>	DATE	3-24-72	
	NEXT HIGHER ASSY			

TITLE

MODERN TEST CONNECTOR

DEC NO.		EIA NO.		SCALE		SHEET		OF		DIST.		SIZE CODE		NUMBER		REV	
												DCS		H315-0-1			



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**DIGITAL EQUIPMENT CORP. DIVISION
MAYNARD, MASSACHUSETTS 01754**

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