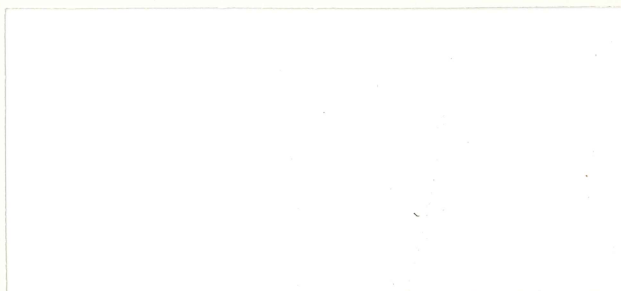


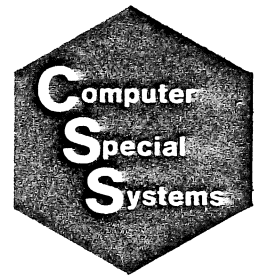
digital

CMS11-K
CARD READER

Computer
Special
Systems

Maynard





CMS11-K
CARD READER

COMPUTER TYPE
PDP-11

DRAWING SET NO.
B-DD-CMS11-K-0

PROGRAM NO.
DECSPEC-11-BBNAD
DECSPEC-11-BBNAX
MAINDEC-11-DZCMF-CA
MAINDEC-11-DZCMF-CB
MAINDEC-11-DZCMF-C01
MAINDEC-11-DZCMF-C02

DOCUMENT NO.
CSS-MO-F-7.1-10A

JUNE 1977

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TABLE OF CONTENTS

1	INTRODUCTION	1-1
1.1	General Description	1-1
1.2	General Operation	1-2
1.3	Specifications	1-3
1.3.1	Mark Sense Card Specifications	1-5
1.4	Physical Description	1-6
2	INSTALLATION	2-1
2.1	Site Considerations	2-1
2.2	Interconnections	2-1
2.2.1	Module Jumpers	2-2
2.3	Card Handling Procedures	2-2
2.3.1	Loading Cards	2-2
2.3.2	Loading and Unloading "ON THE FLY"	2-2
2.3.3	Correcting Error Conditions	2-3
2.4	Initial Operation	2-3
2.4.1	Offline Operation	2-3
2.4.2	Online Operation	2-4
2.5	Checkout Procedure	2-4
2.6	Customer Acceptance	2-5
2.7	Relate Literature	2-5
3	OPERATION AND PROGRAMMING	3-1
3.1	Control and Indicators	3-1
3.2	Card Reader Operation	3-2
3.3	Controller	3-2
3.4	Device Registers	3-4
3.4.1	Status Register	3-5
3.4.2	Data Buffer Register (CRB1)	3-9
3.4.3	Data Buffer Register	3-10
3.4.4	Maintenance Register	3-11
3.5	Interrupts	3-12
4	THEORY OF OPERATION	4-1
4.1	General	4-1
4.2	Address Selection	4-1
4.2.1	Inputs	4-2
4.2.2	Outputs	4-2
4.3	Interrupt Control	4-3
4.4	Status Register	4-5
4.4. 1	Error (Bit 15)	4-5
4.4. 2	Card Done (Bit 14)	4-6
4.4. 3	Hopper Check (Bit 13)	4-6
4.4. 4	Motion Check (Bit 12)	4-6
4.4. 5	Timing Error (Bit 11)	4-7
4.4. 6	Reader To On-Line Transition (Bit 10)	4-8
4.4. 7	Busy (Bit 09)	4-8
4.4. 8	Reader Ready Status (Bit 08)	4-8
4.4. 9	Column Ready (Bit 07)	4-9
4.4.10	Interrupt Enable (Bit 06)	4-9
4.4.11	Eject (Bit 01)	4-10
4.4.12	Read (Bit 00)	4-10
4.5	Data Buffer Register	4-11

4.6	Encoding Network	4-12
4.7	Maintenance Register	4-12
5	MAINTENANCE	5-1
5.1	Special Test Equipment	5-1
5.2	Card Reader Maintenance	5-1
6	CSS BUILT PARTS	6-1
6.1	CSS Built Parts	6-1
Appendix		
A	Shipping List	A-1
A.1	Equipment Furnished	A-1
B	Cable Connections	B-1
B.1	Cable List	B-1
Figures		
1-1		1-2
1-2	Mark Sense Card Specification	1-5
Tables		
1-1	Controller Specifications	1-3
1-2	CR05 Card Reader Specifications	1-4
2-1	Applicable Documents	2-5
3-1	Card Reader Switches And Controls	3-1
4-2	Select Lines + Gating Control Signals	4-3

CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The CMS11-K card reader system is a low cost card handling system designed to interface with the PDP 11 family of processors and peripherals to read marked or punched Hollerith data cards at rates up to 250 @ 60Hz/200 @ 50Hz cards per minute. The CMS11-K system consists of two distinct components: a CR05-C,D,E,F card reader and a DEC PDP-11 interface unit, which is referred to as the controller. Throughout this document all reference to CR05-C,D,E,F card reader will be CR05.

- a. CR05 A motorized card handling device that reads information from EIA (Hollerith) cards. The unit reads 12 row 40 or 80 column cards at a nominal rate of 250 @ 60Hz/200 @ 50Hz cards per minute.
- b. Controller An interface between the card reader and the PDP-11 UNIBUS. Controls data transfers between the card reader and other devices in PDP-11 system. Provides a 12 bit output character for standard data transfers and an 8 bit output character (one byte) when it is desired to use the proposed compressed Hollerith code. Also monitors reader operation And issues appropriate control commands.

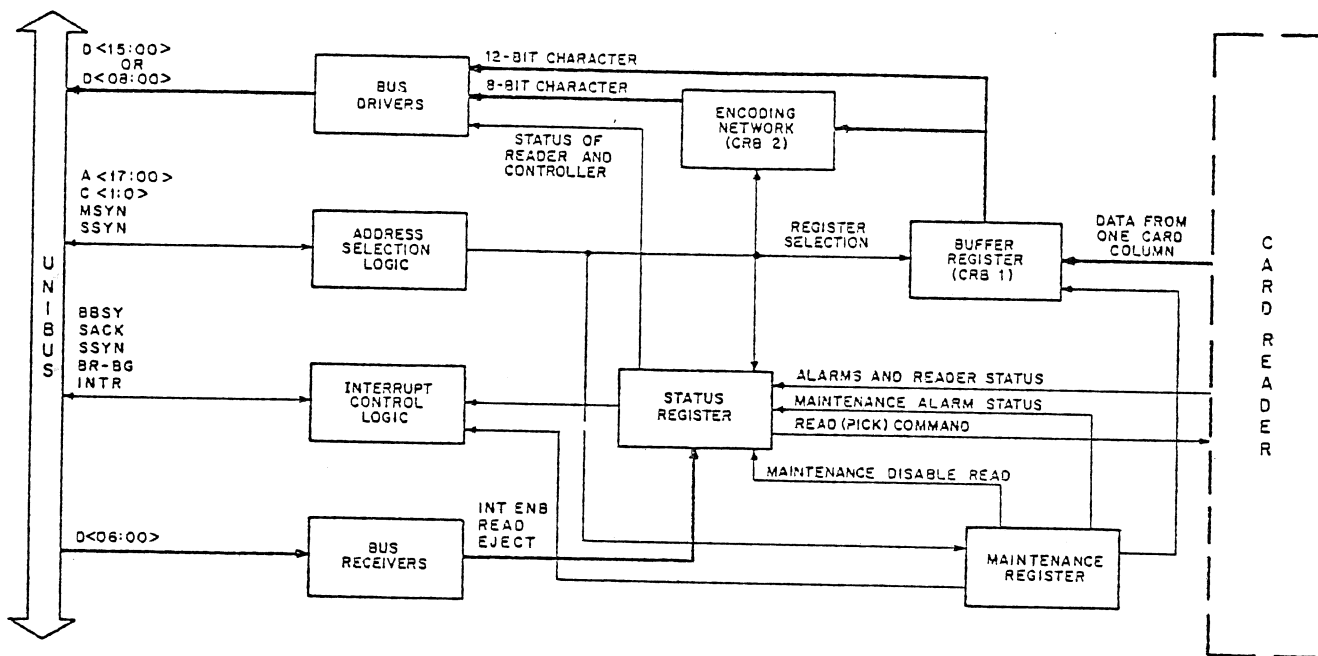


Figure 1-1

1.2 GENERAL OPERATION

A read instruction from the controller moves a card from the input hopper into the read station where all the columns of the card are read on a column-by-column basis beginning with column 1. The card may be read in one of two modes. In the normal mode, data is transferred directly from the rows (zones) of the card to corresponding bit positions in a data buffer for transfer to the bus as a 12 bit character. The bits in this output character correspond directly to zones in the card column.

The second reading mode is the compressed data mode which is compatible with the proposed expansion of the Hollerith code. In this mode, card zones 12 through 08 are transferred directly to the data buffer; however, zones 01 through 07 are encoded into a three bit octal representation before loading into the buffer. This encoding is possible because of the lack of double punched in zones 01 through 07 of both the present and proposed Hollerith codes. As a result of this encoding, the 12 bit data from the card column is compressed into an 8 bit character that is transferred as a low-order byte to the UNIBUS.

Regardless of the reading mode, a punched hole or mark is interpreted as a binary one and the absence of a hole or mark is a binary zero.

1.3 SPECIFICATIONS

Operating and physical specifications for the controller are given in Table 1-1. The specifications for the card reader are given in Table 1-2. The specifications for the mark sense card format are given in Paragraph 1.3.1.

Table 1-1
CONTROLLER SPECIFICATIONS

REGISTERS:	STATUS REGISTER (CRS) DATA BUFFER REGISTER (CRB1) DATA BUFFER REGISTER ENCODED OUTPUT (CRB2) MAINTENANCE REGISTER (CRM)
REGISTER ADDRESSES:	CRS 777160 MAY BE CRB1 777162 CHANGED CRB2 777164 WITH "A" CRM 777166 JUMPERS
DATA OUTPUTS:	CRB1=12 BIT CHARACTER (HOLLERITH CODE) CRB2=8 BIT CHARACTER (COMPRESSED HOLLERITH CODE)
INTERRUPTS:	PRIORITY=BR6 (MAY BE CHANGED BY JUMPER PLUG) VECTOR=LOCATION 230 (MAY BE CHANGED BY "V" JUMPERS) TYPES=ERROR, TRANSITION TO ON LINE, COLUMN READY, AND CARD DONE.
COMMANDS:	READ, AND INTERRUPT ENABLE.
STATUS INDICATORS:	ERROR CONDITIONS=ERROR, CARD SUPPLY ERROR, CARD READER CHECK, TIMING ERROR. OPERATIONAL CONDITIONS=READER READY, READER TRANSITION TO ON-LINE, BUSY, COLUMN READY AND CARD DONE.
SIZE:	THE CONTROLLER CONSISTS OF ONE QUAD MODULE (M8291) THAT OCCUPIES 1/4 OF A DD11 OR ONE SMALL PERIPHERAL CONTROLLER SLOT IN A PDP-11 PROCESSOR SYSTEM UNIT.

POWER: 1.5A @+5V (DERIVED FROM THE POWER
SUPPLY IN THE MOUNTING BOX
IN WHICH THE CONTROLLER IS
INSTALLED)

CABLES STANDARD CABLE IS 25 FEET IN LENGHT
CABLE 7011217-25

Table 1-2
CR05 CARD READER SPECIFICATIONS

CARD TYPE: STANDARD 40 OR 80 COLUMN EIA CARD

LIGHT SOURCE: SINGLE LAMP FIBER OPTICS

READ STATION: PHOTO TRANSISTOR, 12 DATA ROWS AND
1 CLOCK ROW

ELECTRONICS: 7400 SERIES TTL I.C. LOGIC

CARD RATE: 250 CARDS/MINUTE NOMINAL 60HZ
200 CARDS/MINUTE NOMINAL 50HZ

HOPPER/STACKER CAPACITY: 250

POWER: 115 VAC 47-63 HZ, 3.0 AMP NOMINAL
230 VAC 48-52 HZ, 1.5 AMP NOMINAL

DIMENSIONS:

CR05C/D	CR05E/F
HEIGHT: 10.75 INCHES	13.5 INCHES
WIDTH: 19.25 INCHES	19.25 INCHES
DEPTH: 11.75 INCHES	14.75 INCHES
WEIGHT: 32 LBS.	35 LBS.

[illegible]

Figure 1-2
Mark Sense Card Specification

NOTE

1. Trailing edge of clock mark (when used) must coincide with leading edge of marking within $\pm .0025$
2. All preprinting (except clock marks) must be done with reflecting ink (reflective shall be equivalent to that of the card stock)
3. Clock marks (if used) must be printed with non-reflective ink, and should have sharp edges and uniform density.

1.4 PHYSICAL DESCRIPTION

A complete CMS11-K consists of one CR05 card reader, one controller, and one 25 foot cable (7011217-25) to connect the controller to the card reader.

CHAPTER 2

INSTALLATION

2.1 SITE CONSIDERATIONS

The CMS11-K requires one small peripheral controller (SPC) slot either in a DD11 or in the processor of the system in which it will be use.

The card reader is a table top unit and requires an area approximately 20 inches wide and 15 inches deep for normal operation. There should also be sufficient clearance to allow the card reader to be accessed for maintenance purposes.

The card reader is normally supplied with a 25 foot cable which connects to the controller. The location of the reader should take this limitation into account.

No special environmental considerations exist for the CMS11-K. The operating conditions should conform to those for the PDP-11 on which the CMS11-K is to be used.

2.2 INTERCONNECTIONS

The CMS11-K is supplied with one 25 foot signal cable (7011217) which connects to the 40 pin "BERG" connector on the controller module. This cable is routed out of the mounting box and connects to the "ELCO" connector on the rear apron of the card reader.

The power cable of the card reader should be plugged into one of the spare switched outlets in the PDP-11 system. This allows the card reader to be switched ON and OFF with the system power by means of the console power switch of the PDP-11.

2.2.1 MODULE JUMPERS

The address of the CMS11-K interface is determined by ten jumpers on the M8291 module. These jumpers are designated as A03-A12. To set the address for standard device software, remove all but the A03, A07, and A08 jumpers.

The device interrupt vector is also selected by jumpers on the M8291 module. These jumpers, designated V02-V08, must also be set to the desired vector address before the module is seated in the processor. For the standard device software, jumpers V03, V04, and V07 should be left in place, and all the others removed.

There are two other jumpers on the M8291 module which should be checked prior to operation. These are the CR1 and CR2 jumpers which both should be in place. The CM1 and CM2 jumpers should be removed.

2.3 CARD HANDLING PROCEDURES

The following paragraphs present the recommended procedures for loading the input hopper, unloading the output stacker, and correcting error conditions.

2.3.1 Loading Cards

The following procedure is used when loading any deck of cards into the hopper when starting with an empty input hoppers.

1. Fan and rack the cards by hand.
2. Remove the card follower from the input hopper.
3. Place the cards into the input hopper with the column 1 to the left and row 12 toward the front of the reader.
4. Replace the card follower.
5. Press "RESET" and the cards are ready to be read.

2.3.2 Loading And Unloading "ON THE FLY"

The loading and unloading of card "ON THE FLY" is permissible and should offer no problems if a few simple rules are followed:

1. First, since the card follower must be lifted when loading "ON THE FLY", the level of the cards in the input hopper must not be allowed to get below about 100

cards to ensure reliable picking. A convenient gauge for this is the outmost corner on the "TAILS" of the input hopper, which are about 3/4" above the card bed. IE, do not allow the card stack in the input hopper to get lower than about 3/4" in thickness.

2. Secondly, use two hands to unload the output hopper. The procedure that works best is to hold up the cards coming into the hopper with the index finger of the left hand while removing the stack of cards from beneath this finger with the right hand. In removing cards from the output hopper in this fashion, it is recommended that the stack of cards taken at a time be no thicker than about two inches for ease of removal.

2.3.3 Correcting Error Conditions

The RESET switch is illuminated to indicate an error condition, ie. empty hopper, full stacker, pick failure (card read or offline). If while reading cards a HOPPER EMPTY or STACKER FULL error occurs, the RESET lamp will illuminate. In this case, remove the cards from the output stacker or put more cards into the hopper, depending on the obvious condition.

The other indication that an error has occurred is that the RESET indicator will illuminate in the process of reading a deck of cards. When this happens, and the error is not a CARD SUPPLY error, a PICK FAILURE may have occurred. This condition can be either the reader is offline or the inability of the reader to pick the next card ie. a mutilated or card jam. If a card is mutilated or still in the read station, it must be cleared by hand, after which normal operation should be possible again.

2.4 INITIAL OPERATION

All access to internal functions of the card reader should be performed by qualified, trained personnel only.

2.4.1 OFFLINE OPERATION

The CMS11-K user is not provided with offline operation capabilities.

A special offline exercizer (PDI Model 1011 Tester) is provided with the field service spares kit (22-00023-00) to enable offline operation by qualified, trained service personnel.

2.4.2 Online Operation

Once the CR05 is connected to the controller which is installed in the PDP11, the CMS11-K is ready for online operation.

After ascertaining that there are no cards in the hopper, depress the POWER switch. The POWER indicator switch should light, denoting that the power is on. The RESET indicator should illuminate, denoting, in this case, that the input hopper is empty.

Place the cards to be read into the input hopper as described in Paragraph 2.3.1. Select the mode of operation by depressing the MARK/PUNCH switch denoting the format of the cards to be read. Punched cards can be read in the PUNCH or MARK mode, but marked cards can only be read in the MARK mode. Depress the 40/80 COLUMN switch to condition the reader to read 40 or 80 column cards. Depress the INT CLK/CLK TRK switch to select internal timing or the timing marks printed in the "CLOCK TRACKS" of the cards. When CLK TRK mode of operation is selected, the 40/80 COLUMN switch must be in the 80 COLUMN position.

Depress the RESET switch. The RESET indicator lamp should go out, indicating that the check conditions have been satisfied and that the CR05 is now ON-LINE. The controller can now commence to pick cards.

When the input hopper empties, the motor will stop and the RESET indicator will light, denoting that the input hopper is empty and that the CR05 is in the OFFLINE state.

Remove the cards from the output stacker, and if no more cards are to be run, turn off power to the unit by operating the POWER switch.

2.5 CHECKOUT PROCEDURE

The checkout procedure consists of performing the steps in section 2.4.2 prior to running the diagnostic (DECSPEC-11-BBNAD) to insure proper on-line operation. When running the diagnostic as described in the diagnostic writeup, it is necessary to run all tests and to use the four supplied card decks to insure complete checkout of the CMS11-K card reader system. These test decks are:

1. Alpha Test Deck MAINDEC-11-DZCMF-CA
2. Binary Test Deck MAINDEC-11-DZCMF-CB
3. 80 Column Mark Sense MAINDEC-11-DZCMF-C01

4. 40 Column Mark Sense MAINDEC-11-DZCMF-C02

Run punch decks with INT CLK and mark sense decks with CLK TRK.

2.6 CUSTOMER ACCEPTANCE

Customer acceptance consists of running the diagnostic as described in the diagnostic write-up. Three successful passes of all supplied card decks, plus one pass of the error function test (SA 220) are required to fully accept the card reader.

At the customer site, the DECX module, BBNAX, will be incorporated into the system DECX program and run as instructed in the BBNAX listing.

2.7 RELATED LITERATURE

Table 2-1 lists related PDP-11 system documents that are applicable to the CMS11-K card reader system.

Table 2-1
Applicable Documents

Applicable PDP-11 System Manual

Applicable PDP-11 Processor Handbook

PDP-11 Peripherals Handbook

1555 Series Card Reader Operation
and Maintenance Manual from Peripheral
Dynamics Inc.

2022 Series Card Reader Operation and
Maintenance Manual from Peripheral
Dynamics Inc.

CHAPTER 3

OPERATION AND PROGRAMMING

3.1 CONTROLS AND INDICATORS

The control module contains no controls or switches. The controls and indicators for the CMS11-K card reader are given in Table 3-1.

Table 3-1
Card Reader Switches And Controls

POWER	An illuminated alternate action switch which turns the main power to the CR05 ON or OFF.
RESET	An illuminated momentary switch which resets the electronics, and conditions the CR05 to a "READY" condition. The switch is illuminated when the unit is shut down and put offline.
MARK/PUNCH	A white illuminated alternate action switch which when depressed, illuminates to indicate MARK mode, and conditions the electronics to sense MARKS (punched cards may also be read in this mode), or similarly to indicate and read punched cards only.
HALT	A momentary switch, when depressed stops the operation of the reader, and puts it offline to the controller.
40/80 COLUMN	An illuminated alternate action switch conditions the reader to read 40 or 80 column cards. When CLK TRK mode is selected, it remains in the 80 COLUMN position.
INT CLK/CLK TRK	An illuminated alternate action switch which when depressed, alternately conditions the reader to use internal timing or timing marks printed in the "CLOCK TRACKS" of the cards.

3.2 CARD READER OPERATION

The card reader consists of an input hopper for loading a number of cards, a photoelectric read station for reading data from the card, an output stacker for stacking the cards, a motorized mechanism for moving the cards and control and detector logic.

Operation begins with the READ command being issued from the controller. When the reader receives the command, it picks the first card from the hopper and feeds it to the read station. As the data holes or marks pass through the read station, they are sensed by the photoelectric detector. At the same time, the reader generates a series of INDEX or clock marks. These are transmitted to the controller simultaneously with the data bits read from the card. Thus the controller receives 12 bits of parallel data on the 12 data output lines of the card reader and one INDEX mark for each column read.

The card reader generates alarm signals to warn of error conditions present in the reader such as HOPPER EMPTY, STACKER FULL, and PICK FAILURE (reader off-line).

Four program flags indicate the card readers status. These flags are monitored by the controller and are tied to the interrupt logic so that setting any one of these flags generates an interrupt request.

The ON-LINE flag is set whenever the READY line from the card reader goes true indicating that the card reader is ready to accept commands. This feature permits the program to perform other tasks while awaiting manual intervention to clear a card reader problem such as lack of cards in the input hopper. This flag notifies the controller when the card reader is ready to resume on-line operation under program control.

The COLUMN DONE flag requests a program interrupt when a column of data has been read and is ready to be transferred to the bus. The CARD DONE flag is set when the card leaves the read station. The controller should then immediately issue a new READ command to keep the card reader operating at full rated speed. The ERROR flag indicates that an error condition is present in the card reader and an interrupt request is made so that the program can branch to an error-handling routine.

3.3 CONTROLLER

The controller provides the command and monitoring functions for the card reader, in addition to handling data transfers from the card reader to the UNIBUS. When the processor addresses the bus, the controller decodes the address to determine whether the card reader is the selected external device, and if so, whether to perform an input or output operation.

The address selection logic decodes the incoming address and responds to one of four possible sequential addresses. The register that is selected and the type of bus data transfer operation being performed determine whether a command is being issued, status is being monitored, or whether data is being read from a card in one of two reading modes.

If for example, data is to be read, the status register is first addressed so that a READ command can be sent to the card reader. The card reader moves a card into the read station, detects the data from the first card column, and loads it into the buffer register. Once the buffer is loaded, the controller sets a COLUMN READY flag so that an interrupt can be generated to transfer data to the bus.

At this point, either the buffer register (CRB1) or the encoding network (CRB2) would be addressed so that the data, in the form of either a 12-bit or 8-bit character, could be transferred through the bus drivers to the UNIBUS. When CRB1 is addressed, data from the buffer register is applied directly to the bus. When CRB2 is addressed, the 12 bits from the buffer are compressed into an 8-bit character before application to the bus.

When the status register is addressed, it can serve as either a command register to specify certain functions to be performed or as a status register to monitor operations within the controller and the card reader.

When the status register is used as a command register it is loaded from the bus and can perform one or more of the following functions: INTERRUPT ENABLE, READ, or EJECT. INTERRUPT ENABLE is used to condition certain controller circuits so that an interrupt is generated whenever an error occurs, the card reader goes on line, or the reading of a card column or entire card is completed. The READ function is the only command sent to the card reader and is used to start operation of the reader. The EJECT function prevents the COLUMN READY flag from being set so that data from the buffer register is not transmitted to the bus. However, transfers between the card reader and the buffer register still take place. As far as the controller is concerned, the card has been ejected even though the reader still continues normal operation.

When the status register is used to monitor system functions, it operates as a read only register and its output is applied to the bus for monitoring by the program. Some of the bits in the register are set and cleared by alarm and status signals from the card reader itself; other bits are set or cleared by the controller.

The card reader supplies two status signals to the controller: READY, which indicates that the card reader is placed on line; and BUSY which indicates that the reader is currently processing a card. The reader signals an alarm by dropping the READY line, and in the case of a full stacker or empty hopper, it also

presents the HOPPER CHECK alarm, or in the case of a pick failure reader presents the MOTION CHECK alarm.

Status and alarm signals are also generated internally by the controller. These include: ERROR, TIMING ERROR, COLUMN READY, and CARD DONE. TIMING ERROR as indicated by the controller status register is different than the timing error internal to the card reader. The controller TIMING ERROR indicates that a column of data was not read from the buffer by the processor in time and was overwritten by the next column of data.

3.4 DEVICE REGISTERS

The device registers of the controller are listed in Table 3-1. These addresses are standard by can be altered by changing the jumper configuration on the address selection logic. However, any DIGITAL programs or other software referring to these addresses must also be modified accordingly if the jumpers are changed.

Table 3-1
Standard Device Register Assignments

REGISTER	MNEMONIC	ADDRESS
STATUS REGISTER	CRS	777160
DATA BUFFER REGISTER	CRB1	777162
DATA BUFFER REGISTER	CRB2	777164
MAINTENANCE REGISTER	CRM	777166

NOTE

CRB1 is the actual register that holds one column (12 bits) of data from a card (Hollerith code).

CRB2 is the gated output of CRB1 such that the 12-bit buffer output is compressed into an 8-bit character (compressed Hollerith code.)

The DATA BUFFER REGISTER is a read only buffer. It cannot be loaded by the program.

The MAINTENANCE REGISTER is a write only register that cannot be read by the program.

3.4.1 Status Register

15	14	13	12	11	10	09	08	07	06	05	02	01	00
ERR	CARD DONE	HOPPER CHECK	MOTION CHECK	TIMING ERROR	ON-LINE TRANS.	BUSY	READY	COL ROY	INT ENB	UNUSED		EJECT	READ

BIT 15 ERROR

Used to indicate an error condition is present. This bit is set whenever one of the following conditions occur:

1. The card reader goes off-line from an on-line condition. During normal operation, this occurs when a card reader check or supply error is sensed.
2. A TIMING ERROR is present when the reader completes reading of the card (CARD DONE).

If an attempt is made to read a card while the ERROR bit is set and the error causing conditions have not been corrected, the bit remains set and subsequent READ commands are ignored.

This bit is connected to the interrupt logic so that the program can branch to an error handling routine.

This is a read only bit, cleared by INIT.

NOTE

With the error removed, bits 15, 14, 11, and 10 are automatically cleared when the status is loaded. However, if using a DATOB for loading, the low order byte must be used because the high order byte has no effect on the status register.

BIT 14 CARD DONE

When set, indicates that one card has passed through the read station and the next card may be requested from the input hopper. This bit is connected to the interrupt logic.

This is a read only bit, cleared by INIT or by loading the status register.

BIT 13 HOPPER CHECK

When set, this bit indicates that either the input hopper is empty or the output stacker is full. In either case, the condition must be corrected before further operation can take place.

This is a read only bit, cleared by correcting the error condition.

BIT 12 MOTION CHECK

When set, this indicates the presence of a abnormal condition in the card reader. Any one of the following three conditions set this bit:

1. FEED ERROR - indicates the card reader feed mechanisms failed to deliver a card to the read station when demanded.
2. MOTION ERROR - indicates a card jam is the reader.
3. STACK FAIL - indicates that card has not been delivered to the output stacker.

This is a READ ONLY bit cleared by correcting the error condition.

BIT 11 TIMING ERROR

When set, this indicates that a new column of data has been loaded into the data buffer before a previously loaded column was read by the program. Clears COLUMN READY bit at this time and TIMING ERROR causes the ERROR bit to be indicated at CARD DONE time.

Once the TIMING ERROR bit is set, the COLUMN READY flip-flop clocking is inhibited and no data transfers can take place until TIMING ERROR is cleared.

When the EJECT bit is set prior to issuing a READ command, it prevents TIMING ERROR from setting because a timing error is not relevant if the card is ejected.

This is a read only bit, cleared by INIT or by loading that status register.

BIT 10 READER TRANSITION TO ON-LINE

When set, this bit indicates that the card reader has gone on-line and now is under program control. Depressing the card reader RESET switch brings the reader on-line, providing no error conditions exist.

The card reader goes off-line whenever an error condition is sensed or the RESET switch is depressed. When the reader goes from on-line to off-line, the ERROR bit is set.

This bit is connected to the interrupt logic so that the program can identify card reader availability.

This is a read only bit, cleared by INIT or by loading the

status register.

BIT 09 BUSY

When set, indicates that a card is in the process of being read.

This is a read-only bit, cleared when the card is not in the read station or when the READ command is removed.

BIT 08 READER READY STATUS

When set, this bit indicates that the reader is off-line. When clear, indicates the reader is on-line and ready to accept READ commands.

This is a read only bit.

BIT 07 COLUMN READY

When set, indicates that one column of data has been loaded into the data buffer and is ready for transfer to the bus.

When this bit is set and a card is ejected, a TIMING ERROR can still occur if the bit remains set when the new data arrives at the data buffer.

If a card is ejected, COLUMN READY is inhibited from setting.

COLUMN READY is cleared when the data buffer is addressed (either CRB1 or CRB2). This operation does not affect the contents of the data buffer but does clear the COLUMN READY bit.

This bit is also connected to the interrupt logic so that a data transfer can take place once the data has been assembled in the buffer.

This is a read only bit, cleared by INIT or by addressing the data buffer.

BIT 06 INTERRUPT ENABLE

When set, allows an interrupt to occur provided one of the following bits is also set: OFF-LINE (NOT READY), CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY. TIMING ERROR causes an interrupt only when CARD DONE is set.

This is a read/write bit, cleared in INIT.

BITS 05-02 UNUSED

BIT 01 EJECT

When set, this bit prevents the COLUMN READY flag from being set. However, data transfers from the card reader to the data buffer still take place. Although the remaining card columns are actually read by the card reader, absence of COLUMN READY flags make it seem to the controller that the card has been ejected from the read station.

When EJECT is set prior to issuing a READ command, it also prevents the TIMING ERROR bit from being set because a timing error is not relevant if the card is ejected.

Setting EJECT alone does not eject a card. The READ bit must also be set to fetch the card.

This is a read/write bit. cleared by INIT.

BIT 00 READ

When set, this bit causes the card reader feed mechanism to deliver one card to the read station for reading. This bit is always read as a 0.

Cleared by INIT or by loading with a 0. This bit can be loaded by the program, but is always read as a 0 whether set or cleared.

3.4.2 Data Buffer Register (CRB1)

15	12	11	10	09	08	07	06	05	04	03	02	01	00
UNUSED		ZONE 12	ZONE 11	ZONE 10	ZONE 1	ZONE 2	ZONE 3	ZONE 4	ZONE 5	ZONE 6	ZONE 7	ZONE 8	ZONE 9

11-0448

BITS 15-12 UNUSED

BITS 11-00 ZONES 12-1

These bits represent the output of a 12-bit data buffer register. During a read operation, data from a card is loaded into the buffer one column at a time. After each column is loaded, the contents of the buffer is placed on

the UNIBUS for transfer to the processor or other bus device on demand.

When the DATA BUFFER REGISTER is addressed as CRB1 the contents of the buffer is coupled to the 12 least significant bus data lines as follows:

BIT 11=ZONE 12

BIT 10=ZONE 11

BIT 09=ZONE 10

BIT 08=ZONE 01

BIT 07=ZONE 02

BIT 06=ZONE 03

BIT 05=ZONE 04

BIT 04=ZONE 05

BIT 03=ZONE 06

BIT 02=ZONE 07

BIT 01=ZONE 08

BIT 00=ZONE 09

All bits are READ ONLY

3.4.3 Data Buffer Register (CRB2)

15	08	07	06	05	04	03	02	00
UNUSED				ZONE 12	ZONE 11	ZONE 10	ZONE 9	ZONE 8
				OCTAL CODE ZONES 1-7				

11-0449

BITS 15-08 UNUSED

BITS 07-00 ZONES 12-1 COMPRESSED

These bits represent the compressed output of a 12-bit data buffer register. During a read operation, data from a card

is loaded into this buffer one column at a time. After each column is loaded, the contents of the 12-bit buffer are compressed into an 8-bit character by an encoding network and are then gated onto the UNIBUS as a low-order byte. This data compression is made available so that the card reader controller is fully compatible with the proposed expansion of the Hollerith code.

BITS 07-03 are encoded as follows:

BIT 07=ZONE 12

BIT 06=ZONE 11

BIT 05=ZONE 10

BIT 04=ZONE 09

BIT 03=ZONE 08

BITS 02-00 represent an octal code that defines the card zone as shown below. In the case of multiple zones, these bits are in the Inclusive OR of the octal codes of the zones.

BIT 02	BIT 01	BIT 00	CARD ZONE
0	0	0	ZERO (NO PUNCHES IN ANY ZONE FROM 01 TO 07)
0	0	1	ZONE 01
0	1	0	ZONE 02
0	1	1	ZONE 03
0	0	0	ZONE 04
1	0	1	ZONE 05
1	1	0	ZONE 06
1	1	1	ZONE 07

ALL BITS ARE READ ONLY

3.4.4 Maintenance Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MAINT	M BUSY	M RDY	MOT/ HOP	ZONE 12	ZONE 11	ZONE 10	ZONE 1	ZONE 2	ZONE 3	ZONE 4	ZONE 5	ZONE 6	ZONE 7	ZONE 8	ZONE 9

BIT 15 MAINT

When set, this bit allows the processor to check out card reader operation without a card reader being present. Any reference to this register must keep the MAINT bit set or all maintenance functions are disabled.

BIT 14 MBUSY

When set, this bit along with MAINT being set, allows the processor to control the assertion and negation of the BUSY bit on the controller logic.

BIT 13 MRDY

When set, this bit along with MAINT being set, allows the processor to control the assertion and negation of the READ bit in the controller logic.

BIT 12 MOT/HOP

When set, this bit along with MAINT being set, allows the processor to jointly control the assertion and negation of the MOTION and HOPPER CHECK bits in the controller logic.

BITS 11-00 ZONE DATA

When MAINT is set, bits 00-11 simulate data from the card reader. The same bit position assignments used here appear in the CRB1 register.

3.5 INTERRUPTS

The controller uses BR interrupts to gain control of the bus to perform a vector interrupt, thereby causing a branch to a handling routine.

A BR interrupt can occur only if the INTERRUPT ENABLE (IE) bit in the status register is set. When IE is set, an interrupt request

is generated whenever any one of the following bits in the status register is set: READER READY STATUS, CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY.

When the reader READY status bit is set, it indicates that some type of error condition exists. In this case, an interrupt is used to cause a program branch to an error handling routine.

When CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY is set, it indicates that the controller is ready to perform a data transfer or accept a command. In these cases, an interrupt service routine may be used to perform the required operation.

The interrupt priority level is 6 and the interrupt vector address is 230. The priority level can be changed with a priority plug and the vector address can be changed by a different jumper configuration of the M8291 board.

CHAPTER 4

THEORY OF OPERATION

4.1 GENERAL

This section provides a detailed description of the controller module and is divided into five areas: SELECTION LOGIC, INTERRUPT LOGIC, STATUS REGISTER, DATA BUFFER, and COMPRESSED DATA BUFFER.

For complete information on the CR05 card reader, refer to the Peripheral Dynamics Inc. Operation and Maintenance manual applicable to the series model card reader.

For a more complete understanding of the following sections, refer to the block diagram in section 1 of this manual.

4.2 ADDRESS SELECTION

The address selection logic (DRAWING CR-5 on the M8291) decodes the address information from the bus and provides three select lines and two gating signals that determine which register has been selected and whether it is to perform an input or output function. The jumpers on the module are arranged to provide for standard addressing of 777160, 777164, and 777166; all DEC software utilizes these addresses. If a different configuration is made the software must be modified to reflect the change.

The first five digits of the address (77716X) indicate that the controller has been selected as the device to be used. The final digit, consisting of address line A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. The two mode control lines, C0 and C1, determine whether the selected register is to perform an input or output operation.

On the M8291, address lines A02 and A01 are decoded to produce one of four select lines which select the register to be used. The two mode control lines (C1 and C0) produce READ and LOAD gating signals which determine whether the bus cycle is a DATI or DATO.

4.2.1 Inputs

The address selection logic input signals consist of 18 address lines, <A17:A00>; 2 bus control lines, C<1:0>; and a master synchronization (MYSN) line. The address selection logic decodes the incoming address as described below. This address format is shown in Figure 4-2. Note that all input gates are standard bus receivers.

1. Line A00 is used for byte control.
2. Line A01 and A02 are decoded to select one of the four addressable registers; CSR, CRB1, CRB2, MAINT.
3. Decoding of lines A<12:03> is determined by jumpers. When a given line contains a jumper, the address logic searches for a 0 on that line. If there is no jumper, the logic searches for a 1.
4. Address lines A<17:13> must be all ones. This specifies an address within the top 4k byte address bounds in the processor for device registers.

4.2.2 Outputs

The address selection logic outputs signals that are used in the controller permit selection of four 16-bit registers and provide signals used for gating information to and out of the master device. Table 4-2 indicate the input signals that select the control output line states.

Table 4-2
Select Lines + Gating Control Signals

Mode Control	Address Lines	Signal Generated
C<1:0>	A<02:00>	
00	000	READ CRS
10	000	LOAD CRS
00	010	READ CRB1, SEL CRB1
00	100	READ CRB2, SEL CRB2
00	110	SEL. MAINT
10	110	SEL. MAINT, LOAD MAINT

NOTE

1. Lines A<17:13> must be all 1s (0V on Unibus)
2. Lines A<12:03> are selected by jumpers.
3. Gating control signals may become true although select lines are not.

4.3 INTERRUPT CONTROL

The interrupt control logic (drawing CR-5 on M8291) permits the controller to gain control of the bus and perform an interrupt operation. The standard vector address jumper configuration (drawing CR2) is 230 (jumpers in bits V3, V4, and V7); this is the standard configuration. Software modifications must be made for non-standard vector addresses.

The interrupt control logic on the M8291 consists of a single input request and grant acknowledge circuit for establishing bus control.

Before the interrupt control logic can generate an interrupt

request, two input signals must be high: INT A and INT ENB (1)H. The logic that generates these two signals is shown on drawing CR-4 for M8291. When a 1 is loaded into bit 06 of the status register, it sets the INT ENB bit to produce INT ENB (1)H. This signal is applied to the interrupt control logic as an enabling signal on drawing CR-5.

The second signal that must be present to generate an interrupt is INT A H. The INT A H signal is produced by a four input OR gate and is true if any one of the following conditions exists: ERROR, CARD DONE, ONE-LINE, or COLUMN READY.

The master control section of the interrupt logic is used to gain control of the bus. When both the INT A and INT ENB requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the priority plug in the logic. The standard level for the controller is BR6, but this may be changed by the priority plug on the M8291 if desired. When the priority arbitration logic in the processor recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the controller has fulfilled all requirements to become bus master (BBSY false, SSYN false, and BG false), the master control section asserts BBSY.

Once the controller has gained bus control by means of a BR request, an interrupt is generated. The interrupt vector address is selected by jumpers on the M8291 (drawing CR-2). The six selectable lines determines the vector address. An interrupt causes a vector at location 230.

The BG IN signal is allowed to pass through the logic to BUS BG OUT when the controller is not issuing a request. To request bus use, the AND condition of INT A and INT ENB (1)H must be satisfied. These levels must be true until the interrupt service routine clears INT A or INT ENB (1)H. Once bus control has been attained, it is released when the processor has strobed in the interrupt vector. After releasing bus control, the logic inhibits further bus request even if INT A and INT ENB remain asserted. In order to make another bus request, INT A or INT ENB must be dropped and then reasserted to cause the logic to reassert the request line. This prevents multiple interrupts from the same interrupt condition. Note that the interrupt control logic used in the controller is not capable of issuing NPR requests. In order to improve NPR latency, the NPR line is sampled and prevents an interrupt request until all NPR's have been honored.

The sampling of the NPR line is controlled by a jumper (N1) on the controller module. Only certain PDP-11 processors can work with the special circuit described above. The jumper (N1) on the module, when cut, prevents the special circuit from working.

4.4 STATUS REGISTER

The status register is used to monitor operation of both the card reader and the controller and to provide commands to the reader. The status register is a 16-bit register, of which four bits are not used. The following paragraphs describe the circuit logic for each bit used.

4.4.1 Error (Bit 15)

This bit is used to indicate that an error condition is present. There are two conditions that cause an error indication: dropping the card reader READY flag, or the presence of a TIMING ERROR when the reader completes the reading of a card.

The first condition occurs whenever the card reader goes off-line from an on-line condition; in other words, whenever the reader READY flag drops. This error is controlled by an OFF-LINE flip-flop that not only signals an error, but keeps the ERROR bit set if a new command is loaded before the condition that caused the error is corrected.

When the card reader is on-line and in the process of reading a card, the OFF-LINE flip-flop is normally clear. If, however, the card reader READY line goes false (RDY H goes low), then this transition direct sets the OFF-LINE flip-flop. At the same time, the READ flip-flop is held cleared. The output of the ERROR flip-flop passes through an inverter and an OR gate and places a 1 on the bus data line 15 to indicate an error condition when read by the program.

As an example of the operation of the error interlock circuits, assume that the OFF-LINE flip-flop has been set by an ERROR condition, that the ERROR bit has been read but the error has not been corrected by manual intervention at the card reader, and the program is now attempting to load another READ command into the status register.

When a READ command is issued, a 1 is placed on the bus data line 00 which qualifies one leg of a 2-input gate connected to the error bit. The other leg is qualified because the reader READY flag is still down because the error has not been corrected. The output of this gate prevents the clock input from clearing the OFF-LINE flip-flop under these conditions.

Although absence of a READY flag provides a direct clear input to the READ flip-flop, thereby preventing any commands from being transmitted to the reader while the flag is down, the interlock circuit is used to inform the program that an error exists. This is necessary because the program is not able to read that state of the READ flip-flop.

The second condition that can cause an error indication is the

presence of a TIMING ERROR when the reader completes the reading of a card. In this case, the presence of a timing error causes the TIMING ERROR flip-flop to be set and its output is applied to one leg of a 2-input NAND gate. The other leg of the NAND gate is qualified by the output of the CARD DONE flip-flop, which is set when the reading of a card is complete. The output of this NAND gate is applied through the OR gate to bus data line 15 to indicate an error condition exists.

4.4.2 Card Done (Bit 14)

This bit is used to indicate that the reading of one card is complete and that the next card may be requested from the input hopper. The card reader logic indicates card reading complete by dropping the BUSY signal. With two input conditions satisfied (BUSY is negated and the READ flip-flop is cleared), the gate produces a pulsed signal which direct sets the CARD DONE flip-flop.

The output of the CARD DONE flip-flop is tied to the bus data line 14 and to an AND gate in the error logic. The flip-flop output is also applied to the interrupt logic OR gates which produce the INT A H signal so that the interrupt control logic can initiate an interrupt request, provided the INT ENB bit is also set. The purpose of this interrupt request is to allow the controller to issue a new READ command so that a new card can be moved from the input hopper into the read station.

4.4.3 Hopper Check (Bit 13)

This bit is used to indicate the input hopper is empty or the output stacker is full. Manual intervention to correct the condition is required before card reader operation is continued.

The card reader logic produces a supply error signal whenever the hopper is empty or the stacker is full.

4.4.4 Motion Check (Bit 12)

This bit is used to indicate that a pick failure occurred in the card reader. Manual intervention to correct the condition is required before card reader operation is continued. The card reader logic provides the error signal whenever a pick failure occurs.

4.4.5 Timing Error (Bit 11)

This bit is used to indicate a timing error that is the result of loading data into the data buffer before the previously loaded column in the buffer is read by the program.

During normal operation, the card reader generates an INDEX MARKER signal when one complete column of data has been read. This signal is ANDED with the clear side of the TIMING ERROR flip-flop to produce a clock signal. The clock signal is used as a clock for the COLUMN READY flip-flop. Because the two inputs to this flip-flop are both high (EJECT and TIMING ERROR are clear), the clock pulse sets the COLUMN READY flip-flop to indicate card column reading is complete. Although this causes a high to both inputs of the TIMING ERROR flip-flop, it cannot be set until the next clock pulse occurs. However, before the next pulse appears, reading the data registers clears the COLUMN READY flip-flop, removing the high inputs to the TIMING ERROR flip-flop. Clearing the COLUMN READY flip-flop during reading is accomplished by an OR gate connected to the direct clear side of the flip-flop. This OR gate is qualified by reading either of the data registers (CRB1 or CRB2) or by a BUS INITIALIZE.

Assume now that the COLUMN READY flip-flop is set but the DATA BUFFER REGISTER is not read by the program. When the card reader reads the next column and generates the INDEX MARKER signal, another clock signal is produced. In this instance the clock signal sets the TIMING ERROR flip-flop because the two data inputs are still high due to the fact that COLUMN READY was not cleared by reading and is, therefore, still set.

Once the TIMING ERROR flip-flop is set, the COLUMN READY flip-flop is inhibited from setting again after it was cleared by the second INDEX MARK. When TIMING ERROR is set, the clock pulse can no longer be generated because of the AND gate that uses TIMING ERROR (0) H as one of its inputs. Therefore no further data transfers can take place until the TIMING ERROR flip-flop is cleared. The flip-flop can be cleared by BUS INIT or by loading the status register bit 11 with a zero.

If an EJECT command is issued by the controller, it prevents the COLUMN READY flip-flop from setting, which in turn prevents the TIMING ERROR flip-flop from setting. This is done because when a card is ejected, it is not necessary to read any further columns. The program simply waits for a CARD DONE signal then issues a new READ command. The EJECT flip-flop is set by loading a 1 into CSR bit 01. When set, the zero side of the flip-flop goes low, holding one input of the COLUMN READY flip-flop low so that it cannot be set. The TIMING ERROR flip-flop cannot be set because it requires a high signal from the 1 side of COLUMN READY.

4.4.6 Reader To On-Line Transition (Bit 10)

When set, this bit indicates that the card reader has gone on-line and is now under program control. When the RESET switch on the reader is depressed, the card reader goes on-line and produces a READY H signal to the controller. This signal transition is applied to the direct set input of the ON-LINE flip-flop, thereby setting it.

The output of the ON-LINE flip-flop places a logic 1 on the BUS DATA LINE 10 driver and is also applied to the interrupt OR gates to produce the INT A H signal. The controller can now issue an interrupt request (provided INT ENB is set).

If the card reader goes off-line at anytime, the READY H line drops and the gating logic produces a pulsed signal that direct sets the OFF-LINE flip-flop.

4.4.7 Busy (Bit 09)

This bit, when set, indicates that a card is in the process of being read by the card reader. This bit position is controlled by an OR gate that is qualified by either of two conditions; BUSY or READ. Two conditions are necessary because READ is true only while the card is being picked from the hopper and delivered to the read station and BUSY from the card reader is true while the card is being read. Therefore, by using an OR gate for these two conditions, the BUSY bit is a 1 from the time the READ command is issued by the controller until the time card reading is complete, as indicated by the CARD DONE flag.

When the controller issues a READ command, it sets the READ flip-flop. When this flip-flop is set, the 0 side goes low and places a logic 1 on BUS DATA LINE 09. When the card reader receives the READ command, it picks a card, delivers it to the read station, and issues a BUSY signal. The BUSY signal retains a logic 1 on bus data line 09 and the occurrence of the first INDEX MARKER clears the READ flip-flop through an OR gate. The logic 1 remains on the bus data line driver until card reading is complete, at which time the reader drops BUSY. Dropping BUSY causes the data line driver input to return to 0, indicating that the card reader is no longer busy.

4.4.8 Reader Ready Status (Bit 08)

This bit, when set, indicates that the reader is off-line; when clear, it indicates that the card reader is on-line and able to accept commands from the controller.

This bit position is controlled by the READY and the BUSY lines on the M8291. Whenever the READY H signal from the card reader

is true, a controller gate disqualifies the bus driver, causing a logic 0 to be placed on BUS DATA LINE 08. If the READY and BUSY drop on the M8291, the driver is qualified, and a logic 1 is placed on the bus data line driver.

Certain conditions within the card reader must be present before the READY H signal can be true. These conditions are:

1. Power applied and required start-up time completed.
2. Input hopper has been loaded and stacker is not full.
3. No error or abnormal conditions exist.
4. The reset switch has been depressed.

4.4.9 Column Ready (Bit 07)

When set, this bit indicates that one column of data has been read by the card reader, loaded into the controller data buffer, and is ready for transfer to the bus.

The two data inputs to the COLUMN READY J/K flip-flop are from the 0 sides of the TIMING ERROR and EJECT flip-flops. COLUMN READY can never be set if a TIMING ERROR exists or if an EJECT command has been issued. When the card reader completes reading of one column, it generates an INDEX MARKER signal which is gated through the controller logic. This signal clocks the inputs, thereby setting the COLUMN READY flip-flop if no EJECT command has been given.

When set, the output of the COLUMN READY flip-flop places a logic 1 on the BUS DATA 07 driver to indicate data is ready to be transferred. The output also qualifies the interrupt gates to produce INT A H so that the interrupt control logic can initiate an interrupt request, provided the INT ENB bit is also set. The purpose of this interrupt request is to allow the data in the data buffer to be read on to the bus.

The COLUMN READY flip-flop is cleared whenever the data buffer or the data buffer encoding network is addressed. This is accomplished by an OR gate connected to the direct clear input of the flip-flop.

4.4.10 Interrupt Enable (Bit 06)

When set, this bit permits an interrupt to occur provided one of the following bits is also set: ERROR, CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY.

Loading a 1 into status register bit 06 sets the INT ENB flip-flop. The 1 on the data line is the data input to the flip-flop; the clock input is true when the status register has been addressed for loading the low byte. The output of the flip-flop, which is INT ENB H, is applied to one input of an AND gate in the interrupt control logic. The other input to the AND gate is INT A H, which is produced by the interrupt OR gates whenever one of the four conditions mentioned above exists. The INT ENB H signal is also applied to a bus driver to place a 1 on the BUS DATA LINE 06.

The INT ENB flip-flop is cleared by INIT or by loading CSR bit 06 with a 0.

4.4.11 Eject (Bit 01)

When set, this bit indicates that a card is to be ejected (data not transferred to the bus). This is accomplished by preventing the COLUMN READY flip-flop from setting. Although transfers to the bus are inhibited, transfers between the card reader and the controller still take place. Note that setting EJECT does not start card motion; this is accomplished only by the READ bit.

It should be noted that EJECT has no effect on the card reader itself. The reader continues to read the card a column at a time and transfer the data to the DATA BUFFER REGISTER in the controller. Because the buffer is loaded with new data without reading the previous data, a TIMING ERROR should normally occur. This is prevented, however, because the COLUMN READY flip-flop remains clear. A TIMING ERROR indication has no significance during an EJECT operation because the controller has no interest in the data until a CARD DONE flag is set to indicate that the card is out of the read station.

Loading a 1 into the status register bit 01 sets the EJECT flip-flop. The 1 on the data line is the data input to the flip-flop; the clock input is true when the status register is addressed for loading the low byte. When the EJECT flip-flop is set, the 0 side goes low and holds one of the inputs to the COLUMN READY flip-flop low, preventing it from being set. The 1 side of the flip-flop is applied on the BUS DATA LINE 01 driver.

4.4.12 Read (Bit 00)

When set, this bit causes the card reader feed mechanism to deliver to the read station one card for reading. The READ command is the only signal sent to the card reader from the controller.

The data input to the READ flip-flop comes from BUS DATA LINE 00 and is high when a 1 is loaded into this bit position. The clock

signal is true when the status register is addressed for loading the low byte. Thus whenever a 1 is loaded into the bus line 00, the READ flip-flop is set. When set, the 0 side of the flip-flop is inverted and is applied to the card reader as the READ H command.

Unlike other bits in the status register, the READ slip-flop output is not connected to a bus driver for reading. Therefore, this bit position is always read as a 0.

An OR gate connected to the direct clear input of the READ flip-flop enables the flip-flop to be cleared if any one of three conditions occur:

1. A BUS INIT signal is generated.
2. The card reader READY line drops (READY H goes low), indicating that the card reader has gone off-line for some reason.
3. When an INDEX MARK occur.

Note that the READ command is used only to initiate operation of the reader and to cause a card to be moved from the input hopper to the read station. Once actual card reading begins, the READ COMMAND drops and the reader supplies a signal to the controller that signifies it is busy. This signal is BUSY.

4.5 DATA BUFFER REGISTER

During read operations, the DATA BUFFER REGISTER receives and stores the data read by the card reader. Once a complete column is read and stored, the contents of the buffer are placed on the UNIBUS drivers for transfer to the memory or other bus device.

The DATA BUFFER REGISTER consists of 3 SN74298 buffer registers with one, flip-flop corresponding to the zone of a card column. The data input line of each flip-flop is connected to a corresponding data line in the card reader. As the card column is read, the card reader places either a 1 or 0 on the appropriate data line, depending on what is punched in the card.

After the entire column is read and the data has had time to settle, the card reader issues an INDEX MARKER signal. This signal is used by the controller to produce the clock input for each flip-flop. Thus, when the INDEX MARKER is issued by the card reader, a strobe pulse stores the information on the data lines into the corresponding bit position in the buffer register.

In order to read the DATA BUFFER REGISTER, either the register itself (CRB1) or the encoding network (CRB2) must be addressed. When the DATA BUFFER REGISTER (CRB1) is addressed, the data in the 12 flip-flops is gated through to the 12 bus data lines as a

column image.

The clock signal, which was used to load data into the register, is generated by passing the INDEX MARKER signal from the card reader through an AND gate that is qualified only if no TIMING ERROR is present, the clock signal is not generated, and the data register cannot be loaded.

4.6 ENCODING NETWORK

The encoding network is used to compress the 12 bit data character from the card reader to an 8 bit data character that is transferred to the UNIBUS as a low order byte. If the encoding network is selected, data is loaded into the data buffer register in the same manner as before. However, when the bus is addressed for reading, the data is compressed then gate to the bus.

The five most significant bits of the buffer are tied directly to gates representing bus data lines 07-03. The seven least significant bits of the buffer are tied to an encoding network that provides three output lines which are tied to the gates driving BUS DATA LINES 02,01, and 00. The three encoded output lines are COMP D00H, D01H, D02H.

4.7 MAINTENANCE REGISTER

The register consists of a SN74175 buffer which is loaded from the CRM with control bits or data. See section 3.4.4 of this manual for detailed breakdowns of the CRM bits.

The maintenance register of the controller is used only by the diagnostic when no card reader is available, or the CMS11-K has a problem which has to be isolated.

CHAPTER 5

MAINTENANCE

5.1 SPECIAL TEST EQUIPMENT

No special test equipment or tools are required to maintain the controller.

5.2 CARD READER MAINTENANCE

NOTE

All maintenance of the card reader should be performed by trained qualified personnel only.

When problems occur in the use of the CMS11-K it may not be evident as to whether the source of the problems is the card reader or the controller. The diagnostic should be run and the full set of card decks should be run under the control of the diagnostic.

For trouble shooting and maintenance of the card reader refer to the Peripheral Dynamics Inc. Operation And Maintenance Manual.

CHAPTER 6

CSS BUILT PARTS

6.1 CSS PARTS

No CSS special parts are required for this option.

APPENDIX B

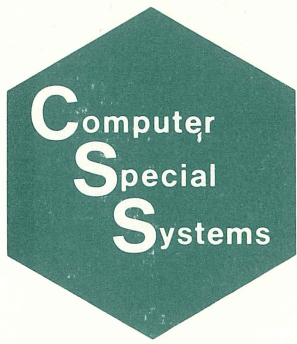
CABLE CONNECTIONS

B.1 CABLE LIST

The following table gives the cable connections for the CMS11-K option.

NAME	PIN NUMBER	TRUE WHEN	PDI
Data bit 12	A	+5 volts if hole	Bit 12
Data bit 12 return	E	GND	Bit 12 ret
Data bit 11	B	+5 volts if hole	Bit 11
Data bit 11 return	F	GND	Bit 11 ret
Data bit 0	C	+5 volts if hole	Bit 0
Data bit 0 return	H	GND	Bit 0 ret
Data bit 1	D	+5 volts if hole	Bit 1
Data bit 1 return	J	GND	Bit 1 ret
Data bit 2	K	+5 volts if hole	Bit 2
Data bit 2 return	P	GND	Bit 2 ret
Data bit 3	L	+5 volts if hole	Bit 3
Data bit 3 return	R	GND	Bit 3 ret
Data bit 4	M	+5 volts if hole	Bit 4
Data bit 4 return	S	GND	Bit 4 ret
Data bit 5	N	+5 volts if hole	Bit 5
Data bit 5 return	T	GND	Bit 5 ret
Data bit 6	U	+5 volts if hole	Bit 6
Data bit 6 return	W	GND	Bit 6 ret
Data bit 7	V	+5 volts if hole	Bit 7
Data bit 7 return	X	GND	Bit 7 ret
Data bit 8	Y	+5 volts if hole	Bit 8
Data bit 8 return	CC	GND	Bit 8 ret
Data bit 9	Z	+5 volts if hole	Bit 9
Data bit 9 return	DD	GND	Bit 9 ret
Data strobe	AA	+5 volts if true	Data Available
Data strobe return	EE	GND	Data Available ret
Ext read command	LL	+5 volts if true	Pick
Ext read command ret	SS	GND	Pick ret
Ready line	BB	+5 volts if true	Motor Status
ready line return	FF	GND	Motor Status ret
Busy	MM	+5 volts if true	Card In Station

Busy return	TT	GND	Card In Station ret
Card supply	JJ	+5 volts if true	Ext Sw.
Card supply return	PP	GND	Ext Sw. ret
Motion Check	KK	+5 volts if true	Pick Failure
Motion Check return	RR	G-D	Pick Failure ret



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