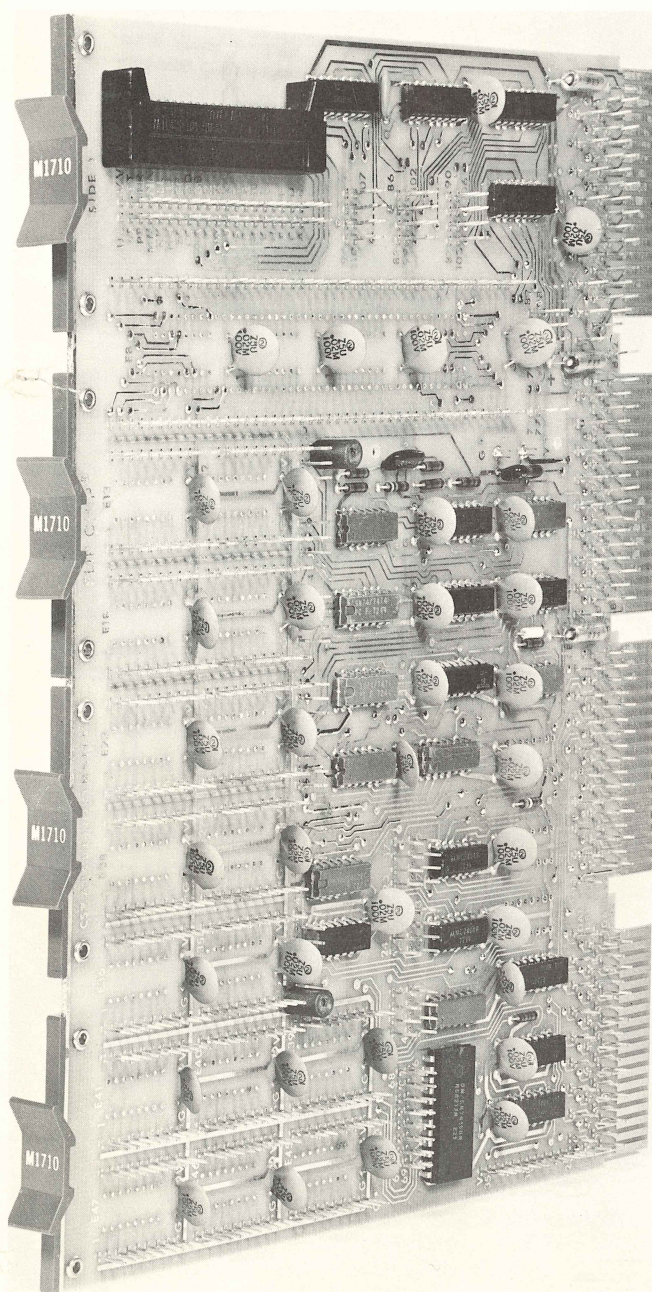


# LOGIC PRODUCTS

APRIL 1974

## M1710 UNIBUS Interface Foundation Module



### DESCRIPTION

The M1710 UNIBUS® Interface Foundation Module is a general-purpose board that provides for the construction of custom interface designs using integrated circuits (ICs). The M1710 lets users build their own interfaces between a wide variety of peripheral equipment and any PDP-11 processor. All essential UNIBUS logic, such as device address selection, interrupt circuitry, and bus receivers and drivers, is provided. In addition, IC mounting pads with wire-wrappable pins are made available for custom logic designs. These pads accommodate all common types of DIP (dual-in-line-package) integrated circuits with up to 40 pins.

The M1710 is a versatile module, ideal for any type of application. The small end user, such as a university laboratory familiar with ICs, will appreciate both the capabilities and cost-effectiveness of the module; no additional mounting panel or power supply is required. These features, coupled with the fact that the M1710 is capable of automatic wire wrapping, also should prove valuable to the large OEM user who requires many custom interfaces. And, in all cases, the module is easily adaptable to accommodate any changes in interface design.

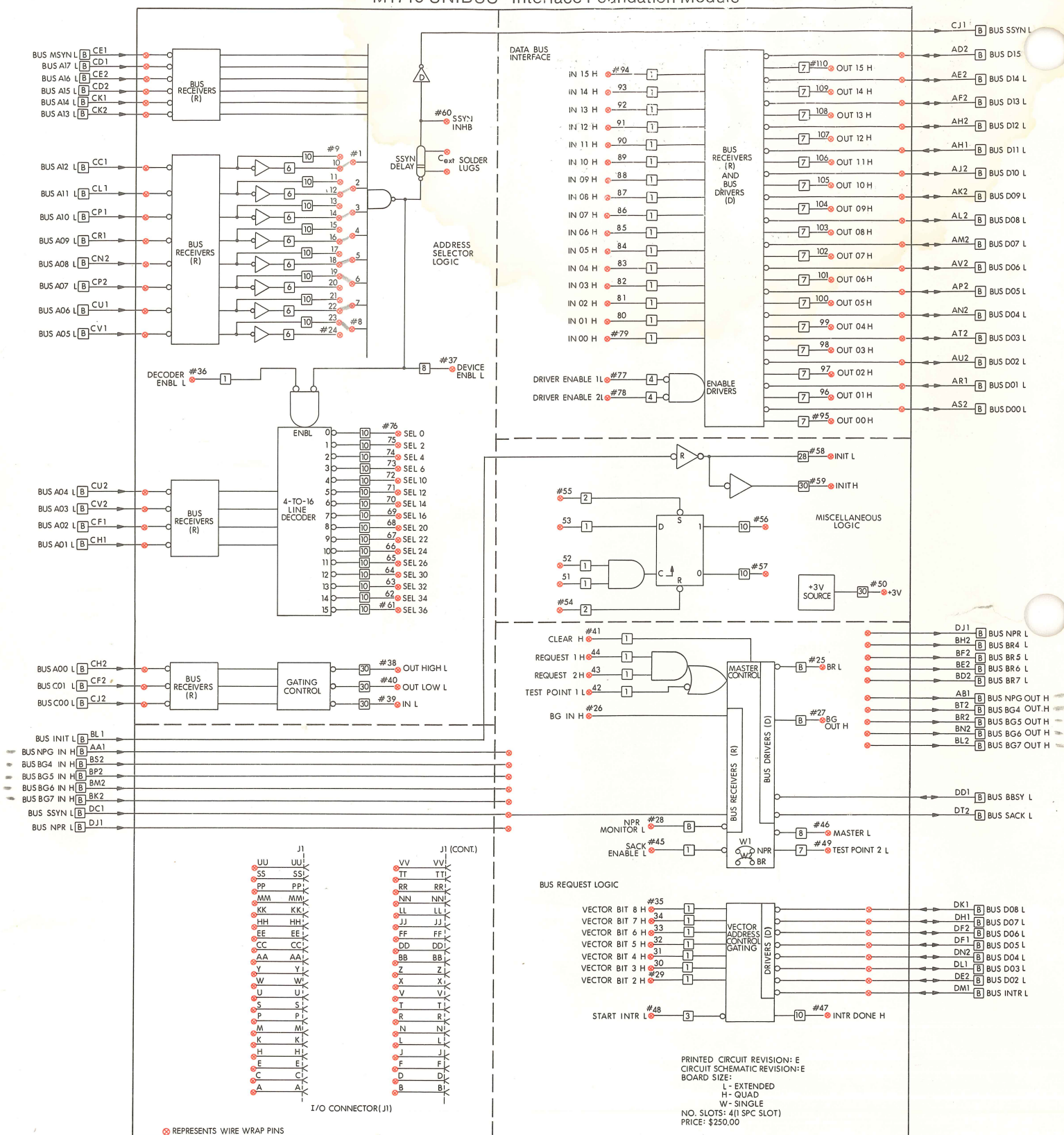
The M1710 plugs into any Small Peripheral Controller (SPC) slot of a DECKit11-M Instrument Interface or DD11 Peripheral Mounting Panel. Additionally, it may be used in a system unit such as the BB11-A. Connection to user equipment is made via a cable that plugs directly into the M1710 module.

### FEATURES

- "Do-it-yourself" interfacing.
- Complete single-card interface.
- Plugs directly into Small Peripheral Controller (SPC) slot.
- Can be used with DECKit11-M Instrument Interface Kit.
- Saves hardware and building costs.
- Preamsembled/pretested UNIBUS circuitry eliminates need to build the required bus interfacing functions.
- Wire-wrappable interconnections—compact, 30-gauge wiring used for all IC lead interconnections.
- I/O connection directly to module board—standard 40-conductor cables available.



## M1710 UNIBUS® Interface Foundation Module



- All accessories and tools available.
- Accepts all common Dual-In-Line Packages (DIPs); mounts up to 16 of the 14- or 16-pin type plus a multi-use pad set that mounts two 40-pin types, three 24-pin types, four 14- or 16-pin types, or combinations of these.
- Additional bus driver and bus receiver ICs available—special high-impedance devices: DEC 8881, DEC 380.
- Includes source of +3 V—convenient for tying unused TTL inputs high, etc.

## APPLICATIONS

Since more and more devices are becoming available in DIP form, quite complex systems can be built on the M1710. Some typical applications include:

- Multiword input and/or output.
- Programmable instrument interfaces.
- Interprocessor buffers.
- Custom peripheral controllers.
- Interfacing of:

- Microprocessors
- A/D converters
- Multiplexers
- Counters
- Shift registers
- ROM and RAM memories
- Arithmetic logic units
- Programmable logic arrays (PLA)

## FUNCTIONS

The M1710 can be divided into four functional sections: address selector logic, bus request logic, data bus interface, and miscellaneous logic. These sections are all shown on the accompanying logic diagram. The logic conventions used on the diagram are explained in the INPUT/OUTPUT SYMBOLOGY section at the end of the data sheet. In addition, note that IN and OUT are always used in respect to the master (controlling) device. Thus, when the M1710 is used in a peripheral device, an OUT transfer is a transfer of data out of the master (such as a processor) and into the device. Likewise, an IN transfer is the operation of the peripheral furnishing data to the master. A detailed discussion of UNIBUS interfacing theory is contained in the *PDP-11 Peripherals Handbook* published by Digital Equipment Corporation.

### Address Selector Logic

The address selector logic provides gating signals for up to 16 full 16-bit device registers. Addresses which can be chosen by the user range from 760000<sub>8</sub> to 777777<sub>8</sub>. The basic M1710 address selection logic is similar in function to the M105 Address Selector Module.

The input signals for the address selector logic consist of: 18 address lines BUS A<17:00>; two bus control lines, BUS C<1:0>; and a master synchronization line, BUS MSYN. The address selector decodes the 18-bit address on lines BUS A<17:00> as described in the following steps. This address format, used for selecting a device register is shown in Figure 1.



Figure 1. Device Register Select Address Format

- Line BUS A00 is used for byte control.
- Lines BUS A<04:01> are decoded by a 4-to-16-line decoder to select one of the 16 addressable device registers. The outputs from this decoder are listed in Table 1.
- Decoding of lines BUS A<12:05> is determined by wire wrap connections on the M1710 module. Both the inverted and noninverted signals are provided at wire wrap pins for each of these eight address lines. Either the inverted (address bit a binary ONE) or noninverted (address bit a binary ZERO) output of each address line must be wired to one of the eight inputs (wire wrap pins 1 through 8) of the address selector AND gate.

Table 1  
Select Line Outputs

Device Register Address Input Lines BUS A<04:01>				Select Signal Output (True=0 V)	Wire Wrap Output Pin
04	03	02	01		
0	0	0	0	SEL 0	#76
0	0	0	1	SEL 2	#75
0	0	1	0	SEL 4	#74
0	0	1	1	SEL 6	#73
0	1	0	0	SEL 10	#72
0	1	0	1	SEL 12	#71
0	1	1	0	SEL 14	#70
0	1	1	1	SEL 16	#69
1	0	0	0	SEL 20	#68
1	0	0	1	SEL 22	#67
1	0	1	0	SEL 24	#66
1	0	1	1	SEL 26	#65
1	1	0	0	SEL 30	#64
1	1	0	1	SEL 32	#63
1	1	1	0	SEL 34	#62
1	1	1	1	SEL 36	#61

- Lines BUS A<17:13> must all be binary ONES. This specifies an address within the top 8K byte address bounds for device registers.



- Control lines BUS C<1:0> are decoded and combined with line BUS A00 to generate the signals IN, OUT LOW and OUT HIGH that must be gated with the select signals to control the direction of data transfer operations. The resultant gating signals from this decoding are listed in Table 2.

**Table 2**  
**Gating Control Signals**

Mode Control BUS C<1:0> C1 C0		Byte Control BUS A00	Gating Control Signal	Transfer Operation Performed	Output Pin
0	0	0	IN	DATI	#39
0	0	1	IN	DATI	
0	1	0	IN	DATIP	
0	1	1	IN	DATIP	
1	0	0	OUT LOW, OUT HIGH	DATO	
1	0	1	OUT LOW, OUT HIGH	DATO	#40 #38
1	1	0	OUT LOW	DATOB	
1	1	1	OUT HIGH	DATOB	

The handshaking operation between the master and the slave device (M1710) is as follows:

The master sends out the address and gating control code to the M1710. After a 150-ns wait (75 ns to allow for signal skew and 75 ns to allow the M1710 to decode the address), the master device sends BUS MSYN L. The address is decoded as described above and, if it is one of the addresses assigned to the M1710, signal BUS SSYN L is asserted following a 100-ns delay. This delay time may be extended to a maximum of 400 ns by adding an external capacitor between the solder lugs provided on the module. Refer to the SPECIAL WIRING/ADJUSTMENTS section of this data sheet for details. When SSYN INHB is grounded, it inhibits the acknowledgment signal BUS SSYN L normally generated by the M1710. In this case, the BUS SSYN L must be generated by another source.

BUS SSYN L indicates the address was recognized and

the data is stored in the M1710 if it is an OUT operation; for an IN operation, BUS SSYN L indicates the address was recognized and data is present on the D lines for transfer to the master. In either case, when the master receives BUS SSYN L, it clears BUS MSYN L. The M1710 receives cleared BUS MSYN L and clears BUS SSYN L. The master, in turn, receives cleared BUS SSYN L which signifies the end of the current transaction; the bus is now free for other use.

The 4-to-16-line decoder logic is enabled at MSYN time if the signal DECODER ENBL L is grounded. This same logic may be disabled or dynamically enabled to allow for the expansion capability of addressing up to 32 16-bit words. Details for this addressing flexibility are provided in the SPECIAL WIRING/ADJUSTMENTS section of this data sheet.

### Bus Request Logic

The M1710 contains the circuitry required to make a bus request and gain control of the bus at either the NPR level or at one of the BR levels. The module also includes circuitry required for transferring a vector address during an interrupt operation. Selection of whether this logic is used for a BR or an NPR level request is explained in the SPECIAL WIRING/ADJUSTMENTS section.

To cause a bus request, whether BR or NPR, both the REQUEST 1 H and REQUEST 2 H inputs must be brought High, causing BR L to be asserted. The particular bus request level is chosen by wire wrapping the BR L output to the proper pin at the bottom of the M1710 that corresponds to one of the BUS BR 4 L through BUS BR 7 L signals. This procedure is described in the SPECIAL WIRING/ADJUSTMENT section.

To acknowledge a bus request, the module must receive the appropriate bus grant signal (BUS BG 4 IN H through BUS BG 7 IN H). The priority level of this grant is the same as the request level and is determined by wire wrapping the BG IN H and BG OUT H signals to the appropriate pins as described in the SPECIAL WIRING/ADJUSTMENTS section.



The BG IN H signal energizes the BUS SACK L output if the particular M1710 is requesting. If the module is not the requesting device, the BG signal will pass through the module and on to the next device via the BG OUT H output.

When the BUS SACK L signal has been sent and the current bus master releases bus control, the M1710 will become the new bus master by asserting BUS BBSY L and MASTER L outputs. Once master, the M1710 can transfer data on the bus. Signal SACK ENABLE L should normally be held High and asserted Low just prior to the last data cycle. BUS SACK L, in turn, will be unasserted as soon as SACK ENABLE L goes Low.

When the M1710 has completed its last data transfer, it can perform either an active or passive bus release if the operation is a BR-type interrupt. A passive bus release is performed by clearing BUS BBSY L and allowing either the processor or another interrupting device to become bus master. If, instead of clearing BUS BBSY L in a passive release, the device asserts BUS INTR L, the processor conducts an interrupt bus transaction called an active bus release.

An active bus release can be performed by tying MASTER L (pin 46) to START INTR L (pin 48). When BUS SACK L is dropped as explained previously, the BUS INTR L output will be activated and the vector address of the interrupt will be placed on the bus data lines, BUS D02L through BUS D08L. This vector address is chosen by wire wrapping logic Highs or Lows on the VECTOR BIT 2 H through VECTOR BIT 8 H inputs. When the processor has accepted the vector address, it returns a BUS SSYN L to the M1710 which now clears BUS INTR L, the vector address, and BUS BBSY L, and releases the bus to the processor, thus completing the interrupt.

When the interrupt is completed, the INTR DONE H can be used to clear the request flip-flop by wiring INTR DONE H to the CLEAR H (pin 41) input. The proper connections necessary for this interrupt circuit are described in the SPECIAL WIRING/ADJUSTMENTS section.

In addition, the single interrupt circuitry on the M1710 can be configured (by adding external gates and flip-flops) to handle two or more interrupting devices, each with a separate vector address.

#### **Data Bus Interface**

The M1710 contains standard UNIBUS receivers which provide a buffered bus signal output for each of the 16 data lines OUT 00 H through OUT 15 H. Output drive capability of these receivers is seven TTL unit loads.

The module also includes 16 bus drivers which drive data lines IN 00 H through IN 15 H. Input loading to each driver is 1.25 standard TTL loads. All 16 drivers have two common gate line enables (DRIVER ENABLE 1 and DRIVER ENABLE 2) which require a logic Low for assertion. Each enable represents four TTL unit loads.

#### **Miscellaneous Logic**

The following additional circuitry is also provided on the M1710:

- Inverted and noninverted buffered INIT outputs (pins 58 and 59) capable of driving 28 and 30 TTL unit loads respectively.
- A general-purpose flip-flop with all input and output pins available for wire wrap (pins 51 through 57).
- A +3-volt source (pin 50) capable of driving 30 TTL unit loads.

## SIGNAL SPECIFICATIONS

For purposes of this data sheet, all signals to and from the M1710 can be categorized into two areas: UNIBUS signals and non-UNIBUS signals.

### UNIBUS Signals

All UNIBUS signals described below conform to specifications outlined in the *PDP-11 Peripherals Handbook*. Refer also to the INPUT/OUTPUT SYMBOLOGY section of this data sheet for loading information.

**BUS MSYN L**—a signal from the master device that initiates the particular M1710 operation and gates in the address and data signals.

**BUS SSYN L**—a signal to the master device indicating the M1710 has received the address and data, and the bus is now free for other operations.

**BUS A00 L through BUS A17 L**—18 lines from the master device to all slaves to determine which slave is to be selected.

**BUS C00, C01**—selects the type of transfer operation.

**BUS D00 L through BUS D15 L**—the 16 bidirectional data lines.

**BUS NPG IN (OUT)**—(Non-Processor Request Grant) the response by the processor to an NPR.

**BUS BG4 IN (OUT) H through BG7 IN (OUT) H**—(Bus Grant) the response by the processor to a BR.

**BUS NPR L**—(Non-Processor Request) a signal from the M1710 to the processor requesting control of the bus for data transfers.

**BUS BR4 L through BR7 L**—(Bus Request) signals from the M1710 requesting control of the bus.

**BUS INTR L**—(Interrupt) a signal from the M1710 (master) to processor to initiate program interruption.

**BUS SACK L**—(Selection Acknowledge) a signal from the M1710 to the processor acknowledging receipt of a BG or NPG.

**BUS BBSY L**—a signal asserted by the master device to indicate bus is being used.

**BUS INIT L**—a clear signal asserted by the PDP-11 when the START key on the console is depressed, when a RESET instruction is executed, or when the power fail sequence occurs.

### Non-UNIBUS Signals

All inputs from external equipment or user-installed IC logic must be standard TTL-compatible levels. All outputs to user-installed IC logic are standard TTL-compatible levels.

**SSYN INHB**—When this input is grounded, it inhibits the acknowledgment signal (SSYN) normally generated by the M1710. In this case, the SSYN must be generated by another source.

**DECODER ENBL L**—When asserted, this signal will permit the 4-to-16-line address decoder to select one of 16 peripheral registers.

**DEVICE ENBL L**—The AND condition of Bus A<05:17> and Bus MSYN. This signal is asserted when one of 16 device registers has been addressed.

**SEL 0 through SEL 36**—Sixteen signals utilized to select one of 16 peripheral registers. Outputs of address decoder.

**CLEAR H**—General reset line used to clear the Bus Request Logic.

**REQUEST 1 H, REQUEST 2 H**—Two signals that are logically ANDed. When both are asserted, a BR or NPR will result.



**TEST POINT 1 L**—External signal that may be asserted to initiate a BR or NPR from the Bus Request Logic.

**BG IN H**—Bus Signal, Processor Arbitration Logic response to a Bus Request.

**SACK ENABLE L**—A signal that will inhibit the clearing of Bus Sack. Used for block transfer DMA cycles.

**MASTER L**—Signal asserted by the Bus Request Logic of the M1710 which indicates the M1710 is the Bus Master.

**TEST POINT 2 H**—This signal is the high-going pulse that is utilized in the M1710's Bus Request Logic to check the Master flip-flop. This signal is for test purposes only.

**START INTR L**—Signal that when asserted will generate a Vector Address and the Interrupt signal to the PDP-11. The signal that initiates the interrupt processes.

**VECTOR BIT 2 H-8 H**—Seven lines that are strobed during the interrupt process to point the processor to the new Program Counter.

**INTR DONE H**—Signal generated by the M1710 when the interrupt process has been completed.

**IN 00 H-IN 15 H**—Sixteen information bits from an external device. Driven by Bus Drivers to the Bus Data lines.

**DRIVER ENABLE 1, 2**—Two signals that when asserted permit the sixteen IN lines to be asserted on the Bus Data lines.

**OUT 00 H-OUT 15 H**—Sixteen information bits that are outputted to an external device. Received by Bus Drivers from the Bus Data lines.

**NPR MONITOR L**—For BR requests, this signal must be connected to the BUS NPR L line. This configuration, if it detects the assertion of the bus grant line to which the module is wired while BUS NPR L is asserted, will block the grant and return BUS SACK L. When the prior bus master has completed its transaction, signal BUS SACK L will be cleared off the bus. The processor will then be able to service the NPR, thus improving the latency time for NPR devices.

## HARDWARE/ACCESSORIES

The M1710 plugs directly into a Small Peripheral Controller (SPC) slot, a DECKit11-M Instrument Interface, or a DD11 Peripheral Mounting Panel.

### Cables

Two cable types are available from DIGITAL in several standard lengths. These cables have the 40-pin (female) mating connector (H856) installed on one or both ends. The part numbers for these two cables are:

**BC07A**—20-conductor twisted pair, H856 connector on one end only; other end is left unterminated to allow unique connections by the user.

**BC08R**—40-conductor flat ribbon, H856 connector on both ends; matches male connector H854 for printed circuit board mounting.

### Wire Wrapping Supplies

Wrapping Tool—H811-A, H810-A, H810-D

Unwrapping Tool—H812-A

30-gauge wire—P/N935

Slip-on patchcords may be used in lieu of wire wrapping for temporary connections. The type 915 patchcord accepts 30-gauge wire-wrap pins and comes in various standard lengths from 2 inches to 64 inches.

All cables, hardware, and wire-wrap tools are described in the 1973-74 *DIGITAL Logic Handbook*.

### Integrated Circuits

DIGITAL makes available the following special integrated circuits for bus interfacing purposes:

DEC 380	High input impedance, 2-input NOR gate IC for receiving UNIBUS signals. Four gates/IC.	P/N 956 \$17.00 Pack of 10 ICs
DEC 8881	Low output leakage current, 2-input NAND gate IC for driving UNIBUS lines. Four gates/IC.	P/N 957 \$19.00 Pack of 10 ICs
	16-pin IC socket, solder-in type.	P/N 954 Pack of 10 sockets \$ 7.00

## SPECIAL WIRING/ADJUSTMENTS

This section describes how to perform the special wiring and adjustments referenced previously in the FUNCTIONS section. All wire wrapping should be performed using 30-gauge solid, insulated wire or, temporarily, with slip-on patchcords. The physical layout of the M1710 is shown in Figure 2 and wire-wrap pin layout is illustrated in Figure 3.

**BUS SSYN Delay Adjustment**—Signal BUS SSYN L is asserted whenever the M1710 is addressed and BUS MSYN L is asserted. There is an approximate 100 ns delay between receiving BUS MSYN L and the assertion of BUS SSYN L to allow for decoding. By incorporating an additional 1000 $\mu$ F capacitor at the solder lugs shown in Figure 2, this delay can be increased to approximately 400 ns.

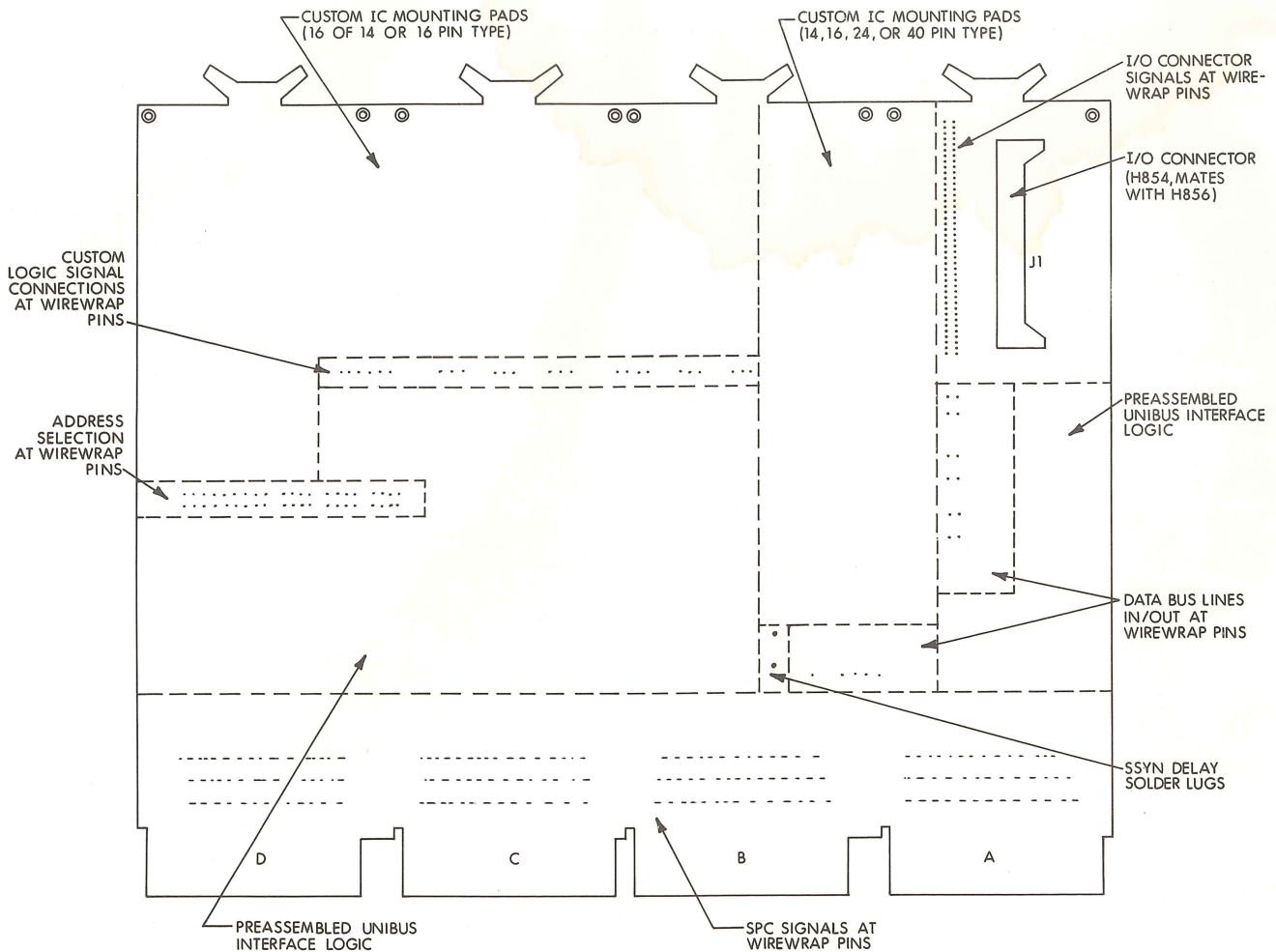


Figure 2. M1710 Physical Layout (Side 1)



● = WIREWRAP PIN  
 G = GROUND  
 V = +5V  
 E = IC NUMBER

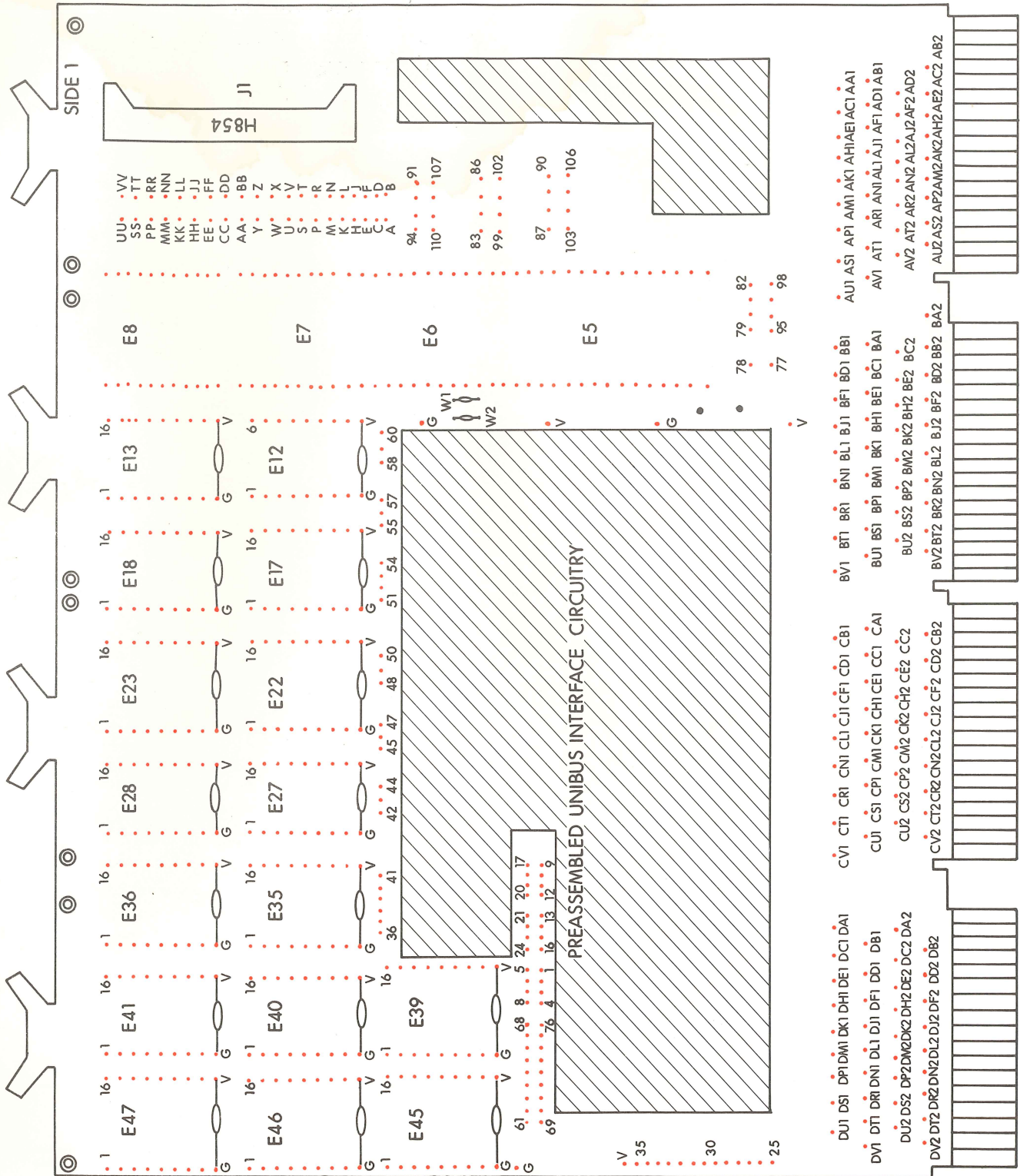
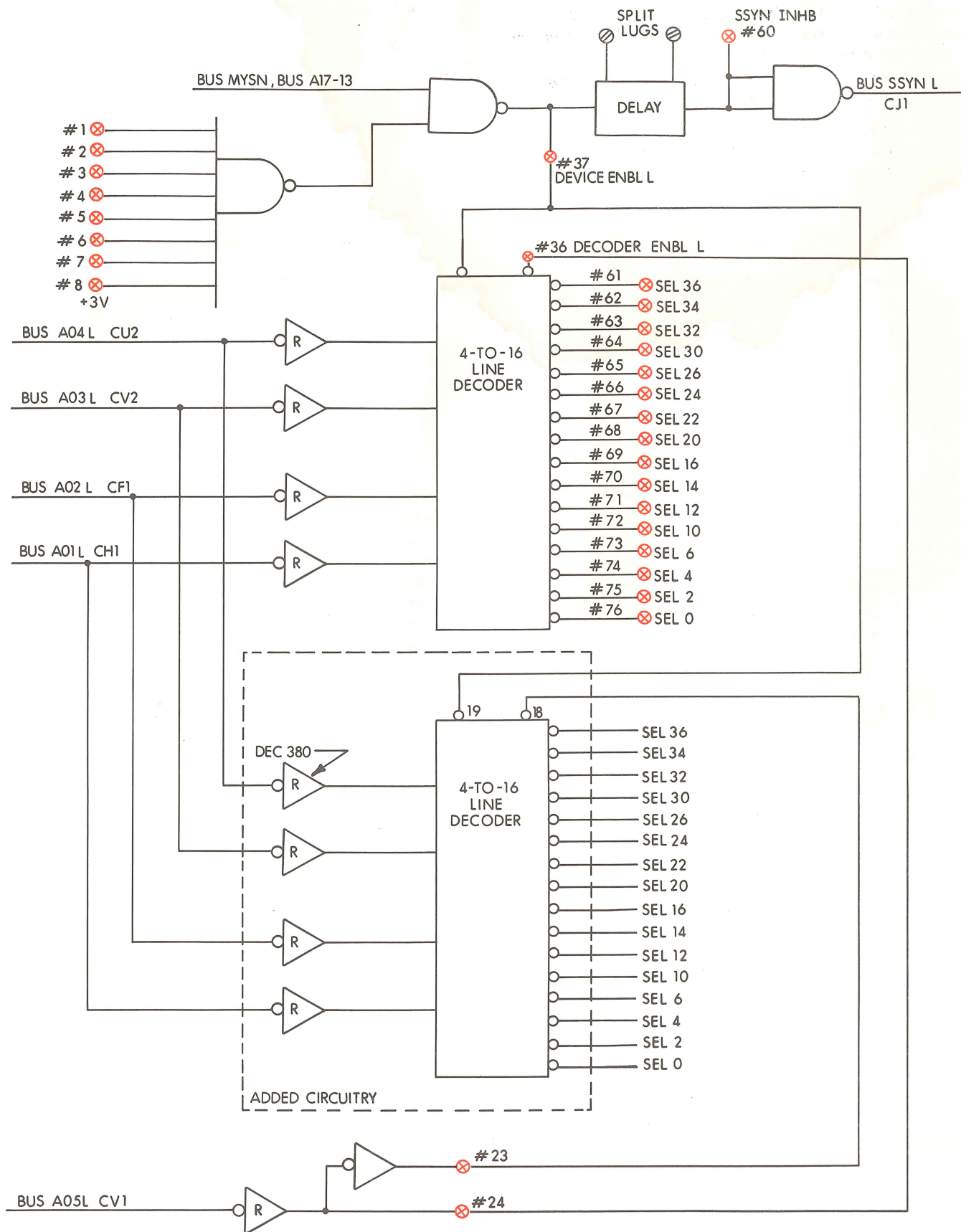


Figure 3. Wirewrap Pin Location Diagram



⊗ REPRESENTS WIRE WRAP PINS

Figure 4. Device Address Expansion Logic



**Device Address Expansion**—By adding the circuitry shown in Figure 4, additional address flexibility can be provided in the M1710. This circuit expansion allows the user to address 32 16-bit device registers.

**NPR or BR Level Request Selection**—There are two types of bus requests: NPR and BR.

For NPR requests, the setup is:

1. Signal NPR MONITOR L tied to +3V source.
2. Jumper W2 removed (jumper W1 must remain inserted).
3. SACK ENBL L is held High until the beginning of the last bus cycle.

Item 1 disables the BUS NPR monitoring circuitry which is not necessary when using this circuit with an NPR device. Item 2 enables the circuitry required for the nonassertion of BUS SACK. Item 3 allows the user to perform multiple word (DMA) transfers during one interrupt cycle.

For BR requests, the setup is:

1. NPR MONITOR L tied to pin DJ1.
2. Jumper W1 removed (jumper W2 must remain inserted).

Item 1 enables the BUS NPR monitoring circuitry which is required when performing BR interrupts. Item 2 enables the circuitry necessary to clear the BUS SACK flip-flop during BR interrupts.

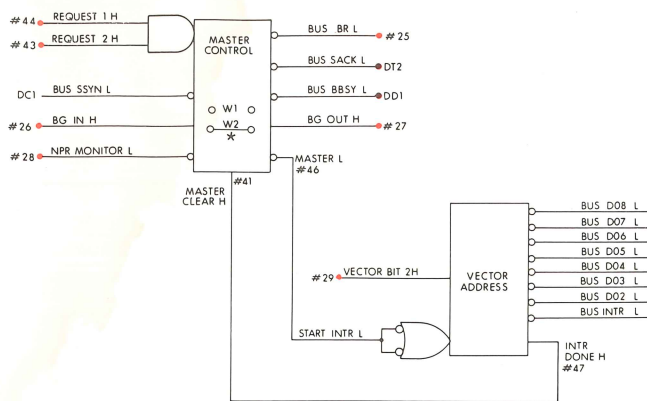
**Bus Request Level Selection**—When generating an interrupt, the appropriate bus request level is chosen by wire wrapping the BR L output to the proper pin at the bottom of the M1710 as follows:

Level	Pin
BR4	BH2
BR5	BF2
BR6	BE2
BR7	BD2
NPR	DJ1

**Bus Grant Level Selection**—The priority level of the grant signal received must be the same as the request level. To accomplish this, the BG IN H and BG OUT H signals must be wire wrapped to one of the following pins

Level	Pin
BG IN 4	BS2
BG IN 5	BP2
BG IN 6	BM2
BG IN 7	BK2
NPG IN	AA1

**Typical Interrupt Circuit**—All of the necessary connections required for the typical interrupt circuit as described earlier in the FUNCTIONS section are shown in Figure 5.



NOTE:  
\* WHEN USED AS A BR DEVICE W2 INSERTED W1 OMITTED  
WHEN USED AS A NPR DEVICE W2 OMITTED W1 INSERTED

Figure 5. Typical Interrupt Circuit Connection

## POWER REQUIREMENTS

All power necessary is provided by the respective PDP-11 processor. The preassembled UNIBUS interface logic uses the following power:

VOLTS	mA TYP	PIN
+5V @ $\pm 5\%$	790	AA2, BA2, CA2
GND		All Pins C, T.

User IC logic also draws its power from the processor supply. Wirewrap pin connections are made available at each IC mounting pad for +5V and GND. The user should calculate the worst case current drain for his custom logic and assure that the processor's supply can accommodate it prior to plugging in the M1710.

## INPUT/OUTPUT SYMBOLOGY

The direction of signal flow on the module diagram is indicated by arrows on the signal lines. Arrows toward the module indicate input signals; arrows away from the module indicate output signals.

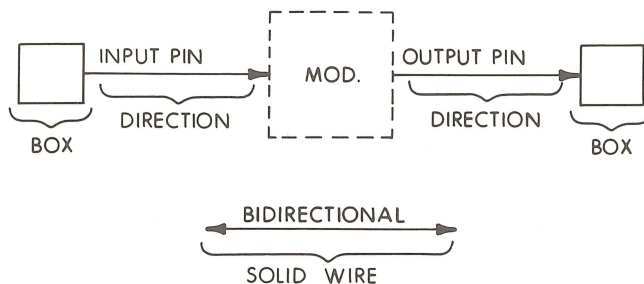


Figure 6. Signal Flow Direction

**Fan-In and Fan-Out**—(in TTL unit loads) is indicated by the number contained in the box associated with each pin. A "B" designation indicates direct connection to the bus.

## Inputs

The loading or designation box always precedes the pin. Symbols with an "R" designation are UNIBUS-compatible receivers.

## Outputs

The loading or designation box always follows the pin. Symbols with a "D" designation are UNIBUS-compatible, open-collector drivers.

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